Integrated Mixed-Signal Solutions

STAC9758/59

High-Performance 6-channel AC97 2.3 CODEC with Universal Jacks™

Datasheet Revision 1.0

2-9758-D1-1-0-0703

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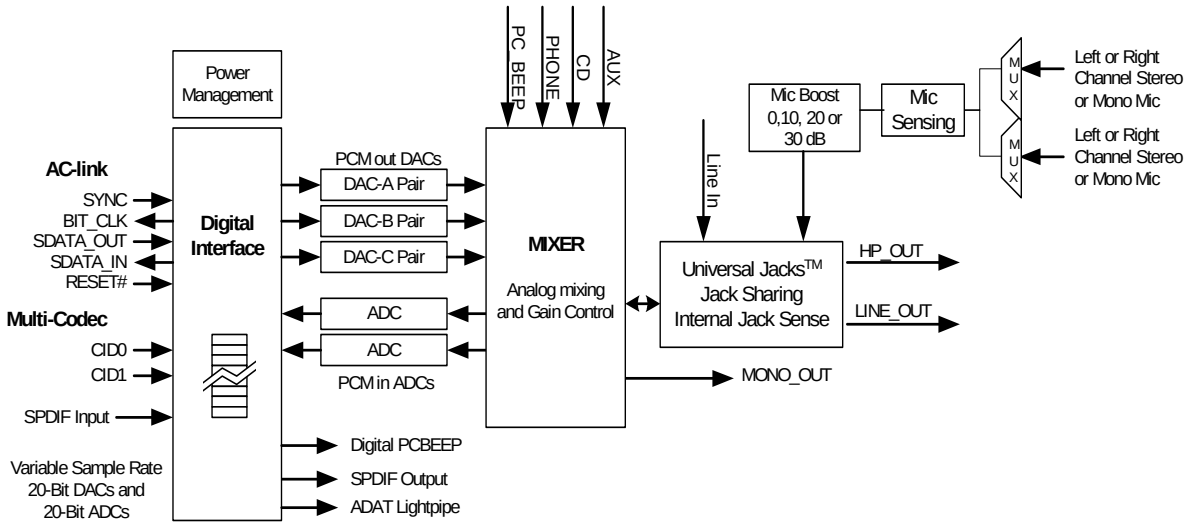
2. PRODUCT BRIEF

- Six Channel, AC'97 Revision 2.3 Compliant
- 20-bit ADCs
- 20-bit DACs
- 96kHz Sample Rate support
- SPDIF OUTPUT at 32kHz, 44.1kHz, and 48kHz
- Double Rate SPDIF Output at 96kHz
- ADAT Optical Lightpipe Output
  - 8 channel, 20 bit output at 48kHz and 44.1 kHz
- SPDIF INPUT at 48kHz and 44.1kHz with Internal Jack Sensing
- HEADPHONE AMPLIFIER with 50mW per channel
- Programmable +3dB voltage gain
- **Universal Jacks™** and 3-jack/6-channel jack-sharing
  - The STAC9758/59 supports 5 stereo analog I/O ports.
  - These ports correspond to the following AC '97 referenced pins: Mic1/2 (21/22), Line_In (23/24), Line_Out (35/36), Surround (39/41), Center/LFE (43/44).
  - These 5 ports may be used in the common "jack sharing" implementation or in a completely reconfigurable ("Universal Jacks™") configuration.
  - Pins 35 and 36 = Headphone (default)
  - Pins 23 and 24 = Line_In (default) or Surround out.
  - Pin 21 and 22 = Mic (default, mono) or CTR/LFE out.
  - Rear jacks are dynamically reconfigurable to input or output.
  - Internal jack sense is used to detect attached devices and inform the driver to reconfigure the jack as appropriate.
  - All "Universal Jacks™" pins (as well as pins 16/17) may also be inputs.
- Mixer Inputs
  - Analog PC Beep, Digital PC Beep, Phone, Aux In, Line In (has pre-select mux for jack sharing/Universal Jacks™), Mic In (mono and stereo modes - includes pre-select mux), DAC-A, DAC-B
  - Split-mute option on all stereo inputs allows left and right inputs to be muted independently.
- Analog Output Sources
  - DAC-A, DAC-B, DAC-C, Stereo Mix, Mono
- Analog I/O
  - Pins 21/22, 23/24, 35/36, 39/41, 43/44
  - All Analog I/O pins have analog jack sense
  - Pins 35/36 and 39/41 are capable of driving headphones
  - All outputs are tri-stated when powered down
- Split-mute (bit D7) option on all outputs allows left and right outputs to be muted independently.
- Internal Microphone Sensing
- Mono and Dual Stereo Microphone Support
- Adjustable VRefOut Control
- Extended AC'97 2.3 Paging Registers

- Up to 5 GPIO depending upon configuration
- Power Management
- SigmaTel SS3D
- Primary and Secondary Mode Operation
- High performance Sigma-Delta technology
- Digital and Analog PC Beep Option
- Digital-ready status
- Crystal Elimination Circuit
- 0, 10db, 20db, and 30 dB microphone boost capability
- +3.3V (STAC9759) and +5V (STAC9758) analog power supply options

2.1. Block Diagram



Ordering Information

Part Number	Package	Temp Range	Supply Range
STAC9758T	48-pin TQFP 7mm x 7mm x 1.4mm	0° C to +70° C	DVdd = 3.3V, AVdd = 5.0V
STAC9759T	48-pin TQFP 7mm x 7mm x 1.4mm	0° C to +70° C	DVdd = 3.3V, AVdd = 3.3V

3. CHARACTERISTICS/SPECIFICATIONS

3.1. Electrical Specifications

3.1.1. Absolute Maximum Ratings:

Voltage on any pin relative to Ground	Vss - 0.3V TO Vdd + 0.3V
Operating Temperature	0 ^{o}C TO 70 ^{o}C
Storage Temperature	-55 ^{o}C TO +125 ^{o}C
Soldering Temperature	260 ^{o}C FOR 10 SECONDS *
VREFOUT Output Current	5mA
Analog Maximum Supply Voltage	6 Volts = AVdd
Digital Maximum Supply Voltage	5.5 Volts = DVdd

***Current package type is not suitable for Lead (Pb) free applications. Please contact SigmaTel if interested in Lead (Pb) free.

3.1.2. Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Power Supplies				
+ 3.3V Digital	3.135	3.3	3.465	V
+ 5V Analog	4.75	5	5.25	V
+ 3.3V Analog	3.135	3.3	3.465	V
Ambient Temperature	0	-	70	^{o}C

ESD: The STAC9758/59 is an ESD (Electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge without detection, electrostatic charges up to 4000 Volts. Even thought the STAC9758/59 includes ESD protection circuitry internally, proper ESD precautions should be followed to avoid damaging the functionality or performance.

3.1.3. Power Consumption *(updated Rev 1.0 release)*

Parameter	Min	Typ	Max	Unit
Digital Supply Current				
+ 3.3V Digital	-	44	-	mA
Analog Supply Current (at Reset state)				
+ 5V Analog	-	58	-	mA
+ 3.3V Analog	-	52	-	mA
Power Down Status (individually asserted) All PR measurements taken while unmuted.				
All paths unmuted +5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	- 96 88 49	-	mA
PR0 +5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	90 82 39	-	mA
PR1 +5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	71 66 34	-	mA
PR2 +5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	51 45 22	-	mA
PR3 +5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	28 26 22	-	mA
PR4 +5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	104 89 1.3	-	mA
PR5 +5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	89 83 22	-	mA
PR6 +5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	84 79 49	-	mA
PR0 & PR1 +5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	- 65 61 22	-	mA
PR0, PR1, PR2, PR6 +5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	- 12 11 22	-	mA
PR0, PR1, PR2, PR3, PR6 +5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	- 0.8 0.6 22	-	mA

Parameter	Min	Typ	Max	Unit
PR0, PR1, PR2, PR3, PR4, PR6 +5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	- 0.8 0.6 1.3	-	mA
For additional power configuration, each SigmaTel DAC pairs can be powered down individually.				

3.1.4. AC-Link Static Digital Specifications

(Tambient = 25 ºC, DVdd = 3.3V ± 5%, AVss=DVss=0V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage Range	Vin	-0.30	-	DVdd + 0.30	V
Low level input range	Vil	-	-	0.35xDVdd	V
High level input voltage	Vih	0.65xDVdd	-	-	V
High level output voltage	Voh	0.90xDVdd	-	-	V
Low level output voltage	Vol	-	-	0.1xDVdd	V
Input Leakage Current (AC-Link inputs)	-	-10	-	10	uA
Output Leakage Current (Hi-Z'd AC-Link outputs)	-	-10	-	10	uA
BIT_CLK (primary mode) Output Leakage Current	-	-10	-	100*	uA
BIT_CLK (secondary mode) Output Leakage Current	-	-10	-	10	uA
Output buffer drive current	-	-	8		mA
BIT_CLK/SPDIF Output Drive Current	-	-	24		mA

* Note: Due to an internal Pull-down resistor, the BIT_CLK pin will exhibit less than 100uA of leakage current when the codec is configured as primary. This pin meets the +/- 10uA leakage specification when configured as secondary.

3.1.5. STAC9758 5V Analog Performance Characteristics

($T_{ambient}$ = 25 ºC, AVdd = 5.0V ± 5%, DVdd = 3.3V ± 5%, AVss=DVss=0V; 1 kHz input sine wave; Sample Frequency = 48 kHz; 0 dB = 1 Vrms, 10KΩ//50pF load, Testbench Characterization BW: 20 Hz – 20 kHz, 0 dB settings on all gain stages)

Parameter	Min	Typ	Max	Unit
Full Scale Input Voltage:				
All Analog Inputs except Mic	-	1.00	-	Vrms
Mic Inputs (Note 1)	-	0.03	-	Vrms
Full Scale Output:				
Line Output	-	1.00	-	Vrms
PCM (DAC) to LINE_OUT	-	1.00	-	Vrms
MONO_OUT	-	1.00	-	Vrms
HEADPHONE_OUT (32Ω load) per channel	-	50	-	mWpk
Dynamic Range: -60dB signal level (Note 2)				
CD to LINE_OUT	-	98	-	dB

Parameter	Min	Typ	Max	Unit
LINE / AUX / VIDEO to LINE_OUT	-	100	-	dB
PCM (DAC) to LINE_OUT	-	85	-	dB
PCM (DAC) in BYPASS Mode to LINE_OUT	-	88	-	dB
LINE_IN to A/D (1VRMS Input Referenced)	-	90	-	dB
LINE_IN to HEADPHONE_OUT	-	94	-	dB
Analog Frequency Response (Note 3)	10	-	30,000	Hz
Total Harmonic Distortion + Noise (-3dB): (Note 4)				
CD to LINE_OUT	-	-90	-	dB
LINE / AUX / VIDEO to LINE_OUT	-	-90	-	dB
PCM (DAC) to LINE_OUT (full scale)	-	-86	-	dB
PCM (DAC) in BYPASS Mode to LINE_OUT	-	-89	-	dB
LINE_IN to A/D(-3dBV input Level)	-	-81	-	dB
HEADPHONE_OUT (32Ω load)	-	-80	-	dB
HEADPHONE_OUT (10k Ω load)	-	-85	-	dB
SNR (idle channel) (Note 5)				
DAC to LINE_OUT	-	85	-	dB
DAC in BYPASS Mode	-	87	-	dB
LINE / AUX / VIDEO to LINE_OUT	-	100	-	dB
LINE_IN to A/D with High Pass Filter enabled	-	92	-	dB
A/D & D/A Digital Filter Pass Band (Note 6)	20	-	19,200	Hz
A/D & D/A Digital Filter Transition Band	19,200	-	28,800	Hz
A/D & D/A Digital Filter Stop Band	28,800	-	-	Hz
A/D & D/A Digital Filter Stop Band Rejection (Note 7)	-100	-	-	dB
DAC Out-of-Band Rejection (Note 8)	-55	-	-	dB
Group Delay (48KHz sample rate)	-	-	1	ms
Power Supply Rejection Ratio (1kHz)	-	-70	-	dB
Power Supply Rejection Ratio (20kHz)	-	-40	-	dB
Any Analog Input to LINE_OUT Crosstalk (10KHz Signal Frequency)	-	-70	-	dB
Any Analog Input to LINE_OUT Crosstalk (1KHz Signal Frequency)	-	-90	-	dB
Spurious Tone Rejection	-	-100	-	dB
Attenuation, Gain Step Size	-	1.5	-	dB
Input Impedance	-	50	-	KΩ
Input Capacitance	-	15	-	pF
VREFout	-	0.5 X AVdd	-	V
VREF	-	0.45X AVdd	-	V
Interchannel Gain Mismatch ADC	-	-	0.5	dB

Parameter	Min	Typ	Max	Unit
Interchannel Gain Mismatch DAC	-	-	0.5	dB
Gain Drift	-	100	-	ppm/ºC
DAC Offset Voltage	-	10	20	mV
Deviation from Linear Phase	-	-	1	deg.
LINE_OUT/MONO_OUT Load Resistance	10	-	-	KΩ
LINE_OUT/MONO_OUT Load Capacitance	-	-	50	pF
HEADPHONE_OUT Load Resistance	-	32	-	Ω
HEADPHONE_OUT Load Capacitance	-	-	100	pF
Mute Attenuation	-	96	-	dB
PLL lock time	-	100	200	usec
PLL 24.576MHz clock jitter	-	-	750	psec
PLL frequency multiplication tolerance	-	-	12.5	ppm
PLL bit clock jitter	-	-	750	psec

Note:
1. With +30 dB Boost on, 1.00 Vrms with Boost off.
2. Ratio of Full Scale signal to noise output with -60dB signal, measured “A weighted” over a 20 Hz to a 20 kHz bandwidth.
3. ± 1dB limits for Line Output & 0 dB gain, at -20dBV
4. Ratio of Full Scale signal to THD+N output with -3dB signal, measured “A weighted” over a 20 Hz to a 20 kHz bandwidth. 48 kHz Sample Frequency
5. Ratio of Full Scale signal to idle channel noise output is measured “A weighted” over a 20 Hz to a 20 kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
6. Peak-to-Peak Ripple over Passband meets ± 0.25dB limits, 48 kHz Sample Frequency.
7. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
8. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 kHz, with respect to a 1 Vrms DAC output.

3.1.6. STAC9759 3.3V Analog Performance Characteristics

($T_{ambient}$ = 25 ºC, AVdd = DVdd = 3.3V ± 5%, AVss=DVss=0V; 1 kHz input sine wave; Sample Frequency = 48 kHz; 0 dB = 1 Vrms, 10KΩ//50pF load, Testbench Characterization BW: 20 Hz – 20 kHz, 0 dB settings on all gain stages)

Parameter	Min	Typ	Max	Unit
Full Scale Input Voltage:				
All Analog Inputs except Mic	-	1.00	-	Vrms
Mic Inputs (Note 1)	-	0.03	-	Vrms
Full Scale Output:				
Line Output	-	0.5	-	Vrms
PCM (DAC) to LINE_OUT	-	0.5	-	Vrms
MONO_OUT	-	0.5	-	Vrms
HEADPHONE_OUT (32Ω load) per channel	-	12.5	-	mWpk
Dynamic Range: -60dB signal level (Note 2)				
CD to LINE_OUT	-	85	-	dB

Parameter	Min	Typ	Max	Unit
LINE / AUX / VIDEO to LINE_OUT	-	85	-	dB
PCM (DAC) to LINE_OUT	-	82	-	dB
PCM (DAC) in BYPASS Mode to LINE_OUT	-	83	-	dB
LINE_IN to A/D	-	85	-	dB
LINE_IN to HEADPHONE_OUT	-	85	-	dB
Analog Frequency Response (Note 3)	10	-	30,000	Hz
Total Harmonic Distortion + Noise (-3dB): (Note 4)				
CD to LINE_OUT	-	-90	-	dB
LINE / AUX / VIDEO to LINE_OUT	-	-92	-	dB
PCM (DAC) to LINE_OUT (full scale)	-	-81	-	dB
PCM (DAC) in BYPASS Mode to LINE_OUT	-	-84	-	dB
LINE_IN to A/D(-3dBV input Level)	-	-81	-	dB
HEADPHONE_OUT (32Ω load)	-	-80	-	dB
HEADPHONE_OUT (10k Ω load)	-	-90	-	dB
SNR (idle channel) (Note 5)				
DAC to LINE_OUT	-	83	-	dB
DAC in BYPASS Mode	-	86	-	dB
LINE / AUX / VIDEO to LINE_OUT	-	100	-	dB
LINE_IN to A/D with High Pass Filter enabled	-	88	-	dB
A/D & D/A Digital Filter Pass Band (Note 6)	20	-	19,200	Hz
A/D & D/A Digital Filter Transition Band	19,200	-	28,800	Hz
A/D & D/A Digital Filter Stop Band	28,800	-	-	Hz
A/D & D/A Digital Filter Stop Band Rejection (Note 7)	-100	-	-	dB
DAC Out-of-Band Rejection (Note 8)	-55	-	-	dB
Group Delay (48KHz sample rate)	-	-	1	ms
Power Supply Rejection Ratio (1kHz)	-	-70	-	dB
Power Supply Rejection Ratio (20kHz)	-	-40	-	dB
Any Analog Input to LINE_OUT Crosstalk (10KHz Signal Frequency)	-	-70	-	dB
Any Analog Input to LINE_OUT Crosstalk (1KHz Signal Frequency)	-	-90	-	dB
Spurious Tone Rejection	-	-100	-	dB
Attenuation, Gain Step Size	-	1.5	-	dB
Input Impedance	-	50	-	KΩ
Input Capacitance	-	15	-	pF
VREFout	-	0.5 X AVdd	-	V
VREF	-	0.41X AVdd	-	V
Interchannel Gain Mismatch ADC	-	-	0.5	dB

Parameter	Min	Typ	Max	Unit
Interchannel Gain Mismatch DAC	-	-	0.5	dB
Gain Drift	-	100	-	ppm/ºC
DAC Offset Voltage	-	10	20	mV
Deviation from Linear Phase	-	-	1	deg.
LINE_OUT/MONO_OUT Load Resistance	10	-	-	KΩ
LINE_OUT/MONO_OUT Load Capacitance	-	-	50	pF
HEADPHONE_OUT Load Resistance	-	32	-	Ω
HEADPHONE_OUT Load Capacitance	-	-	100	pF
Mute Attenuation	-	96	-	dB
PLL lock time	-	100	200	usec
PLL 24.576MHz clock jitter	-	-	750	psec
PLL frequency multiplication tolerance	-	-	12.5	ppm

Note:
1. With +30 dB Boost on, 1.00 Vrms with Boost off.
2. Ratio of Full Scale signal to noise output with -60dB signal, measured “A weighted” over a 20 Hz to a 20 kHz bandwidth.
3. ± 1dB limits for Line Output & 0 dB gain, at -20dBV
4. Ratio of Full Scale signal to THD+N output with -3dB signal, measured “A weighted” over a 20 Hz to a 20 kHz bandwidth. 48 kHz Sample Frequency
5. Ratio of Full Scale signal to idle channel noise output is measured “A weighted” over a 20 Hz to a 20 kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
6. Peak-to-Peak Ripple over Passband meets ± 0.25dB limits, 48 kHz Sample Frequency.
7. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
8. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 kHz, with respect to a 1 Vrms DAC output.

3.2. AC Timing Characteristics

($T_{ambient}$ = 25 °C, AVdd = 3.3V or 5V ± 5%, DVdd = 3.3V ± 5%, AVss=DVss=0V; 50pF external load)

3.2.1. Cold Reset

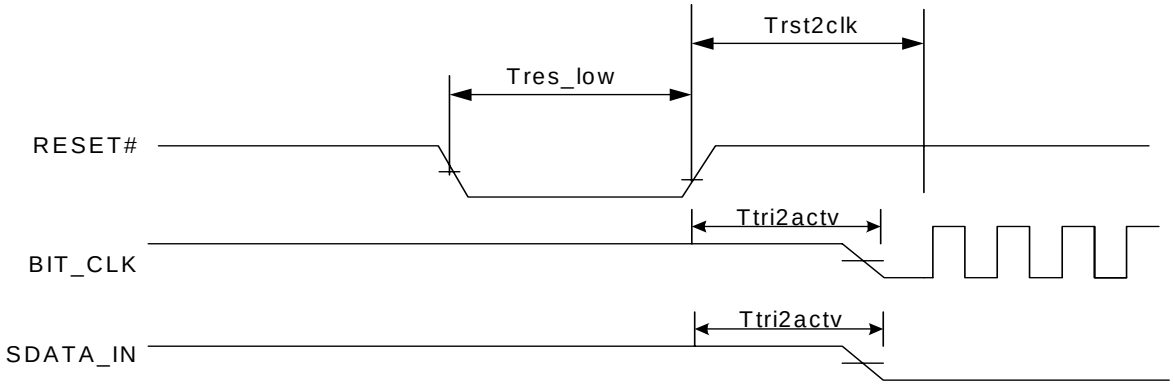


Figure 1. Cold Reset Timing

Parameter	Symbol	Min	Typ	Max	Units
RESET# active low pulse width	Tres_low	1.0	-	-	us
RESET# inactive to SDATA_IN or BIT_CLK active delay	Tri2actv	-	-	25	ns
RESET# inactive to BIT_CLK startup delay	Trst2clk	0.1628	-	400	us
BIT_CLK active to RESET# asserted	Tclk2rst	0.416	-	-	us

Note: BIT_CLK and SDATA_IN are in a high impedance state during reset.

3.2.2. Warm Reset

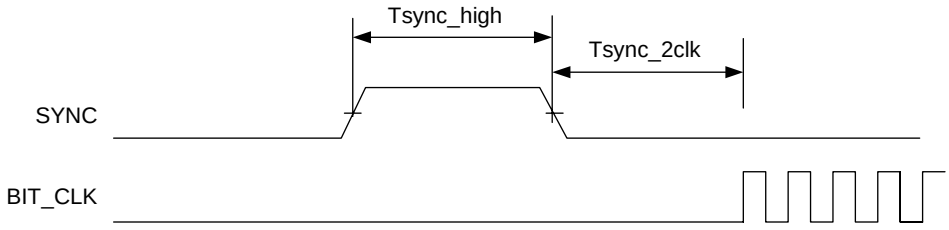


Figure 2. Warm Reset Timing

Parameter	Symbol	Min	Typ	Max	Units
SYNC active high pulse width	Tsync_high	1.0	1.3	-	us
SYNC inactive to BIT_CLK startup delay	Tsync2clk	162.8	-	-	ns

3.2.3. Clocks

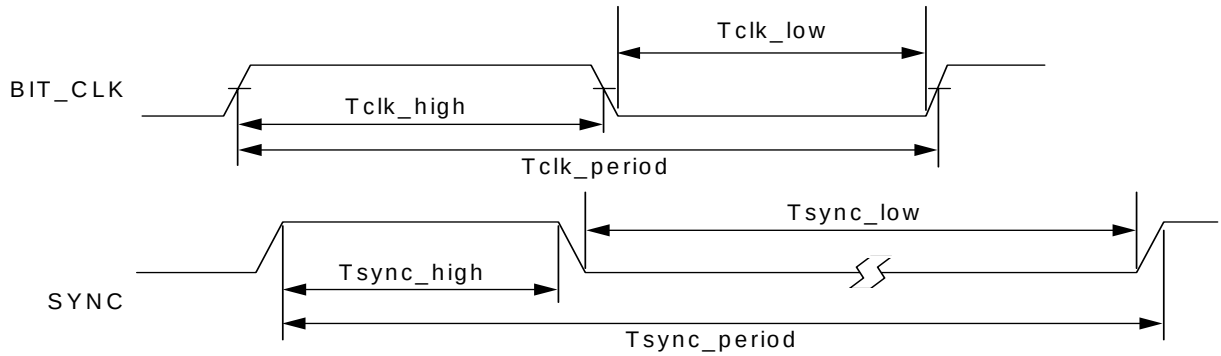


Figure 3. Clocks Timing

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	Tclk_period	-	81.4	-	ns
BIT_CLK output jitter		-	750	-	ps
BLT_CLK high pulsewidth (Note 1)	Tclk_high	36	40.7	45	ns
BIT_CLK low pulse width (Note 1)	Tclk_low	36	40.7	45	ns
SYNC frequency		-	48.0	-	kHz
SYNC period	Tsync_period	-	20.8	-	us
SYNC high pulse width	Tsync_high	-	1.3	-	us
SYNC low_pulse width	Tsync_low	-	19.5	-	us

Note: 1. Worst case duty cycle restricted to 45/55.

3.2.4. STAC9758/59 Crystal Elimination Circuit and Clock Frequencies

The STAC9758/59 supports several clock frequency inputs as described in the following table. In general, when a 24.576MHz xtal is not used, the xtalout pin should be tied to ground. This short to ground configures the part into an alternate clock mode and enables an on board PLL.

Codec Modes:

P = The STAC9758/59 as a Primary Codec

S = The STAC9758/59 as a Secondary Codec

XTL_OUT pin config	CID1 pin config	clock source input	Codec mode	codec ID
xtal	float	24.576MHz xtal	P	0
short to ground	float	14.31818MHz source	P	0
short to ground	pulldown	48MHz source	P	0
XTAL or open	pulldown	12.288MHz bit clk	S	2

Table 1. Clock mode configuration

Whenever pin 3 is pulled down, the codec will be in primary mode with the codec ID 0 regardless of the state of CID1 pin. The only secondary mode operation available is with external device sourcing BIT_CLK and codec ID=2.

Clock Source	Clock Frequency
XTAL	24.576MHz
BIT_CLK	12.288MHz
VGA	14.31818MHz
USB	48MHz

Table 2. Common Clocks and Sources

Note:

1) Pin #2 (Crystal_In) may be left unconnected if codec is in secondary mode.

3.2.5. *Data Setup and Hold*

(50pF external load)

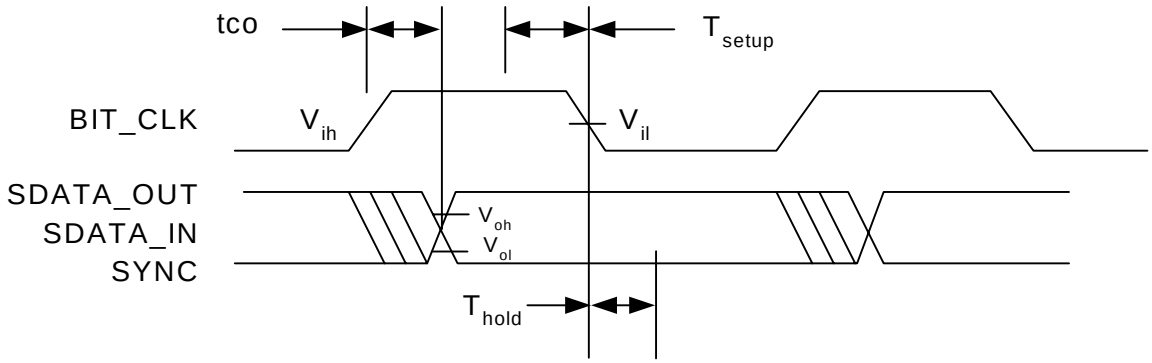


Figure 4. Data Setup and Hold Timing

Parameter	Symbol	Min	Typ	Max	Units
Setup to falling edge of BIT_CLK	Tsetup	10	-	-	ns
Hold from falling edge of BIT_CLK	Thold	10	-	-	ns

Note: Setup and hold time parameters for SDATA_IN are with respect to the AC'97 controller.

3.2.6. *Signal Rise and Fall Times*

(BIT_CLK: 75pF external load; from 10% to 90% of Vdd)

(SDATA_IN: 60pF external load; from 10% to 90% of Vdd))

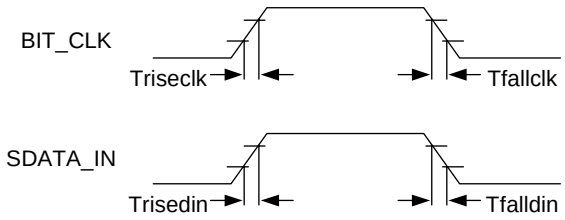


Figure 5. Signal Rise and Fall Times Timing

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK rise time	Triseclk	-	-	6	ns
BIT_CLK fall time	Tfallclk	-	-	6	ns
SDATA_IN rise time	Trisedin	-	-	6	ns
SDATA_IN fall time	Tfalldin	-	-	6	ns

3.2.7. AC-Link Low Power Mode Timing

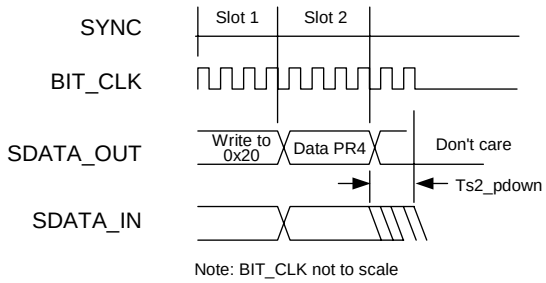


Figure 6. AC-Link Low Power Mode Timing

Parameter	Symbol	Min	Typ	Max	Units
End of Slot 2 to BIT_CLK, SDATA_IN low	Ts2_pdown	-	-	1.0	us

3.2.8. ATE Test Mode

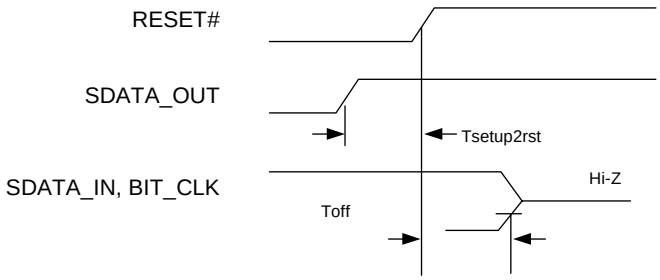
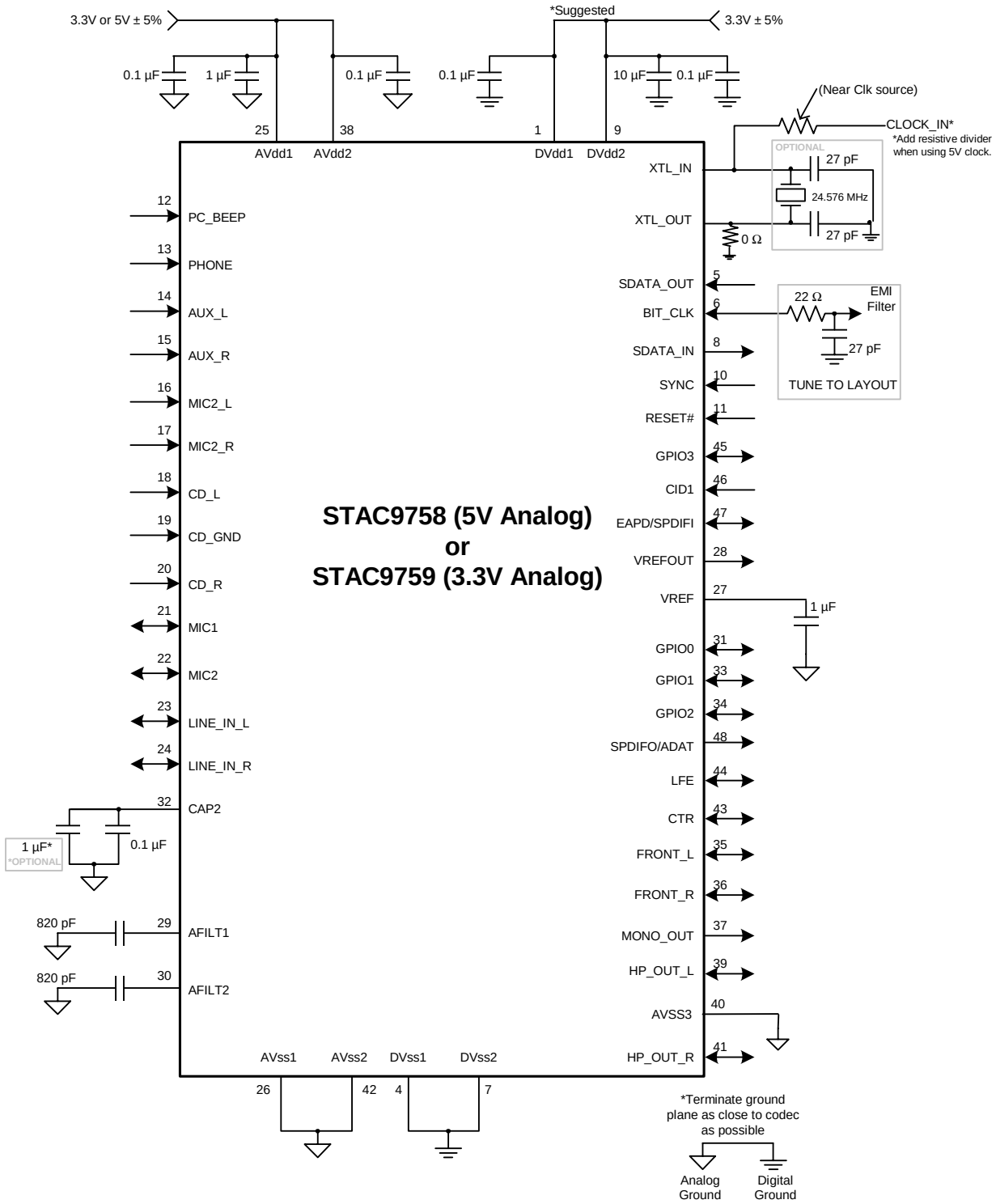


Figure 7. ATE Test Mode Timing

Parameter	Symbol	Min	Typ	Max	Units
Setup to trailing edge of RESET# (also applies to SYNC)	Tsetup2rst	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	Toff	-	-	25.0	ns

Note:
1. All AC-Link signals are normally low through the trailing edge of RESET#. Bringing SDATA_OUT high for the trailing edge of RESET# cause the STAC9758/59 AC-Link outputs to go high impedance which is suitable for ATE in circuit testing.
2. Once the test mode has been entered, the STAC9758/59 must be issued another RESET# with all AC-Link signals low to return to the normal operating mode.
3. # denotes active low.

4. TYPICAL CONNECTION DIAGRAM



See the Reference Design for additional connection information.

NOTE: If pin 48 is held high at powerup, this bit will be held to zero, to indicate the SPDIF is not available. Tie to ground with a 10K resistor to ensure SPDIF is enabled.

Figure 8. Typical Connection Diagram

4.1. SPLIT INDEPENDENT POWER SUPPLY OPERATION

In PC applications, one power supply input to the STAC9758/59 may be derived from a supply regulator and the other directly from the PCI power supply bus. When power is applied to the PC, the regulated supply input to the IC will be applied some time delay after the PCI power supply. Without proper on-chip partitioning of the analog and digital circuitry, some manufacturer's codecs would be subject to on-chip SCR type latch-up.

SigmaTel's STAC9758/59 specifically allows power-up sequencing delays between the analog (AVddx) and digital (VDddx) supply pins. These two power supplies can power-up independently and at different rates with no adverse effects to the codec. The IC is designed with independent analog and digital circuitry that prevents on-chip SCR type latch-up. See the Reference Design for additional connection information.

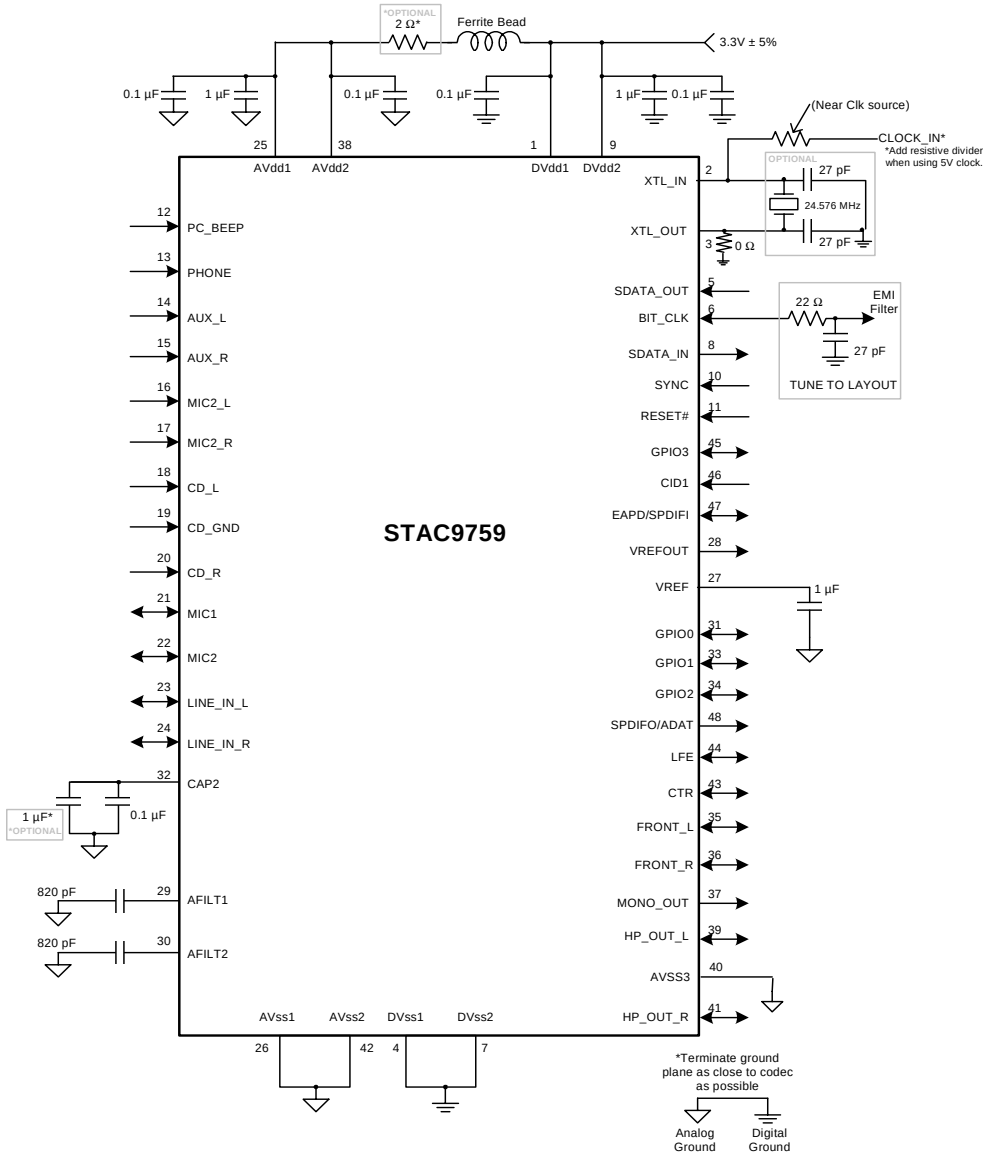


Figure 9. Split Independent Power Supply Operation

NOTE: If pin 48 is held high at powerup, this bit will be held to zero, to indicate the SPDIF is not available. Tie to ground with a 10K resistor to ensure SPDIF is enabled.

5. CONTROLLER, CODEC, AND AC-LINK

This section describes the physical and high-level functional aspects of the AC ‘97 Controller to Codec interface, referred to as AC-link.

5.1. AC-link Physical interface

The STAC9758/59 communicates with its companion Digital Controller via the AC-link digital serial interface. AC-link has been defined to support connections between a single Controller and up to four Codecs. All digital audio, modem, and handset data streams, as well as all control (command/status) information are communicated over this serial interconnect, which consists of a clock (BIT_CLK), frame synchronization (SYNC), serial data in (SDATA_IN), serial data out (SDATA_OUT), and a reset (RESET#).

5.2. Controller to Single Codec

The simplest and most common AC ‘97 system configuration is a point-to-point AC-link connection between Controller and the STAC9758/59, as illustrated in Figure 10.

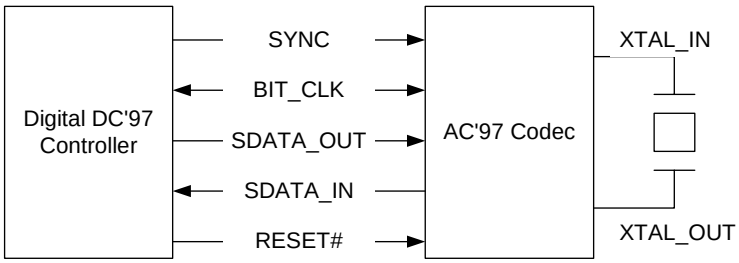


Figure 10. AC-Link to its Companion Controller

A primary codec may act as either a source or a consumer of the bit clock, depending on the configuration.

While RESET# is asserted, if a clock is present at the BIT_CLK pin for at least five cycles before RESET# is de-asserted, then the codec is a consumer of BIT_CLK, and must not drive BIT_CLK when RESET# is de-asserted. The clock is being provided by other than the primary codec, for instance by the controller or an independent clock chip. In this case the primary codec must act as a consumer of the BIT_CLK signal as if it were a secondary codec.

This clock source detection must be done each time the RESET# line is asserted. In the case of a warm reset, where the clock is halted but RESET# is not asserted, the codec must remember the clock source, and not begin generating the clock on the assertion of SYNC if the codec had previously determined that it was a consumer of BIT_CLK.

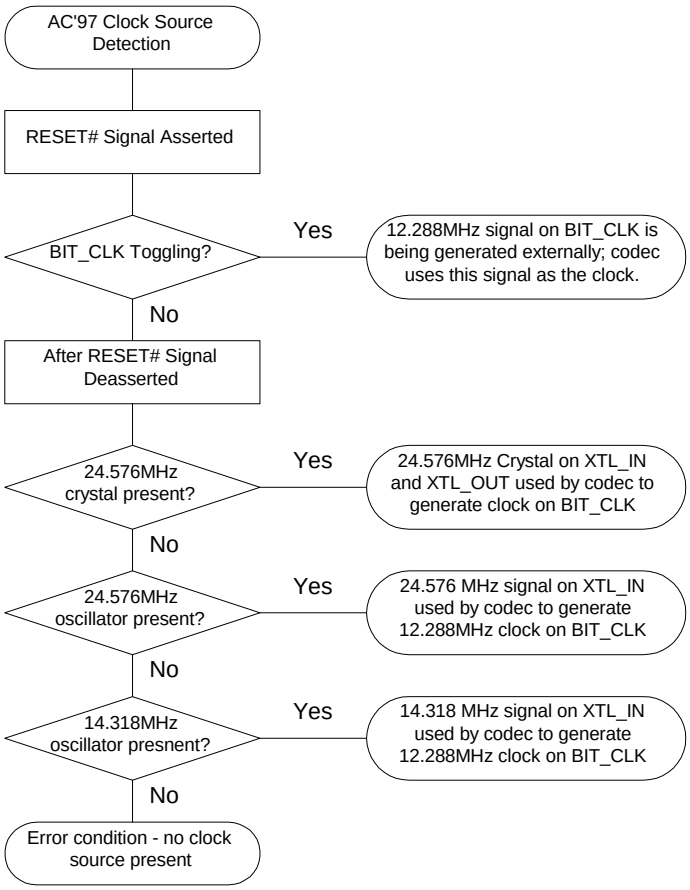


Figure 11. Codec Clock Source Detection

The STAC9758/59 uses the XTAL_OUT Pin (Pin 3) and the CID0 and CID1 pins (Pins 45 & 46) to determine its alternate clock frequencies. See section 3.2.4: page 18 for additional information on Crystal Elimination and for supported clock frequencies.

If, when the RESET# signal has been de-asserted, the codec has not detected a signal on BIT_CLK as defined in the previous paragraph then the AC ‘97 Codec derives its clock internally from an externally attached 24.576 MHz crystal or oscillator, or optionally from an external 14.318MHz oscillator, and drives a buffered 12.288MHz clock to its digital companion Controller over AC-link under the signal name “BIT_CLK”. Clock jitter at the DACs and ADCs is a fundamental impediment to high quality output, and the internally generated clock will provide AC ‘97 with a clean clock that is independent of the physical proximity of AC ‘97’s companion Digital Controller (henceforth referred to as “the Controller”).

If BIT_CLK begins toggling while the RESET# signal is still asserted, the clock is being provided by other than the primary codec, for instance by the controller or by a discrete clock source. In this case, the primary codec must act as a consumer of the BIT_CLK signal as if it were a secondary codec.

The beginning of all audio sample packets, or Audio Frames, transferred over AC-link is synchronized to the rising edge of the SYNC signal. SYNC is driven by the Controller. The Controller generates SYNC by dividing BIT_CLK by 256 and

applying some conditioning to tailor its duty cycle. This yields a 48 kHz SYNC signal whose period defines an audio frame. Data is transitioned on AC-link on every rising edge of BIT_CLK, and subsequently sampled by the receiving device on the receiving side of AC-link on each immediately following falling edge of BIT_CLK.

5.3. Controller to Multiple Codecs

Several vendor specific methods of supporting multiple Codec configurations on AC-link have been implemented or proposed, including Codecs with selective AC-link pass-through and controllers with duplicate AC-links.

Potential implementations include:

- 6-channel audio using 3 x 2-channel Codecs
- Separate Codecs for independent audio and modem AFE
- Docking stations, where one Codec is in the laptop and another is in the dock

This specification defines support for up to four Codecs on the AC-link. By definition there can be one Primary Codec (ID 00) and up to three Secondary Codecs (IDs 01,10, and 11). The Codec ID functions as a chip select. Secondary devices therefore have completely orthogonal register sets; each is individually accessible and they do not share registers.

Multiple Codec AC-link implementations must run off a common BIT_CLK. They can potentially save Controller pins by sharing SYNC, SDATA_OUT, and RESET# from the AC '97 Digital Controller. Each device requires its own SDATA_IN pin back to the Controller. This prevents contention of multiple devices on one serial input line.

Support for multiple Codec operation necessitates a specially designed Controller. An AC '97 Digital Controller that supports multiple Codec configurations implements multiple SDATA_IN inputs, supporting one Primary Codec and up to three Secondary Codecs.

5.3.1. Primary Codec Addressing

Primary AC '97 Codecs respond to register read and write commands directed to Codec ID 00 for details of the Primary and Secondary Codec addressing protocols. Primary devices must be configurable (by hardwiring, strap pin(s), or other methods) as Codec ID 00, and reflect this in the two-bit Codec ID field(s) of the Extended Audio and/or Extended Modem ID Register(s).

The Primary Codec may either drive the BIT_CLK signal or consume a signal provided by the digital controller or other clock generator.

5.3.2. Secondary Codec Addressing

Secondary AC '97 Codecs respond to register read and write commands directed to Codec IDs 01, 10, or 11. Secondary devices must be configurable (via hardwiring, strap pin(s), or other methods) as Codec IDs 01, 10, or 11 in the two-bit field(s) of the Extended Audio and/or Extended Modem ID Register(s).

Codecs configured as Secondary must power up with the BIT_CLK pin configured as an input. Using the provided BIT_CLK signal is necessary to ensure that everything on the AC-link is synchronous. BIT_CLK is the clock source (multiplied by 2 so that the internal rate is 24.576 MHz).

5.3.3. Codec ID Strapping

Audio Codecs in the 48-pin package use pins 45 and 46 (defined as ID0# and ID1#) as strapping (i.e. configuration) pins to configure the Codec ID. The ID0# and ID1# strapping bits adopt inverted polarity and default to 00 = Primary (via a weak internal pullup) when left floating. This eliminates the need for external resistors for Codecs configured as Primary, and maintains backward compatibility with existing layouts that treat pins 45 and 46 as "no connect" or cap to ground. Pulldowns are typically 0-10 kΩ and connected to Digital (not Analog) Ground.

The STAC9758 is normally operated as Primary, which ID 00. Pin 46 is used as CID1. Pin 45 is used as GPIO3.

XTAL_OUT (pin 3)	Pin 46)	Pin 45	Configuration
short to gnd	NA (Freq Select)	NA (GPIO3)	Primary ID 00
XTAL	NC	NA (GPIO3)	Primary ID 00
XTAL	pulldown	NA (GPIO3)	Secondary ID 01

Table 3. Recommended Codec ID strapping

5.4. Clocking for Multiple Codec Implementations

To keep the system synchronous, all Primary and Secondary Codec clocking must be derived from the same clock source, so they are operating on the same time base. In addition, all AC-link protocol timing must be based on the BIT_CLK signal, to ensure that everything on the AC-link will be synchronous.

As a Secondary Codec, the STAC9758 uses the Primary's BIT_CLK output to derive 24.576 MHz.

See section 3.2.4: page 18 for clock frequencies supported and configurations.

5.5. STAC9758/59 as a Primary Codec

The following clocking options are supported as a primary:

- 24.576 MHz crystal attached to XTAL_IN and XTAL_OUT
- 24.576 MHz external oscillator provided to XTAL_IN
- 14.318 MHz external oscillator provided to XTAL_IN
- 48 MHz external oscillator provided to XTAL_IN

See section 3.2.4: page 18 for clock frequencies supported and configurations.

5.5.1. STAC9758/59 as a Secondary Codec

The following clocking options are supported as a secondary:

- BIT_CLK input provided by the Primary. In this mode, a clock at XTAL_IN (Pin 2) is ignored and may be left unconnected.

See section 3.2.4: page 18 for clock frequencies supported and configurations.

5.6. AC-link Power Management

5.6.1. Powering down the AC-link

The AC-link signals can be placed in a low power mode. When AC '97's Powerdown Register (26h) is programmed to the appropriate value, both BIT_CLK and SDATA_IN are brought to and held at a logic low voltage level. After signaling a reset to AC '97, the AC '97 Controller should not attempt to play or capture audio data until it has sampled a Codec Ready indication from AC '97.

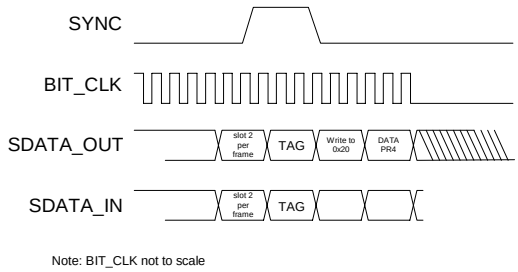


Figure 12. STAC9758/59 Powerdown Timing

BIT_CLK and SDATA_IN are transitioned low immediately following decode of the write to the Powerdown Register (26h) with PR4. When the AC '97 Controller driver is at the point where it is ready to program the AC-link into its low power mode, slots 1 and 2 are assumed to be the only valid stream in the audio output frame.

After programming the AC '97 device to this low power, halted mode, the AC '97 Controller is required to drive and keep SYNC and SDATA_OUT low.

Once the AC '97 Codec has been instructed to halt BIT_CLK, a special "wake-up" protocol must be used to bring the AC-link to the active mode since normal audio output and input frames can not be communicated in the absence of BIT_CLK.

5.6.2. Waking up the AC-link

There are two methods for bringing the AC-link out of a low power, halted mode. Regardless of the method, it is the AC '97 Controller that performs the wake-up task.

5.6.2.1. Controller Initiates Wake-up

AC-link protocol provides for a "Cold AC '97 Reset", and a "Warm AC '97 Reset". The current powerdown state would ultimately dictate which form of AC '97 reset is appropriate. Unless a "cold" or "register" reset (a write to the Reset Register) is performed, wherein the AC '97 registers are initialized to their default values, registers are required to keep state during all powerdown modes.

Once powered down, re-activation of the AC-link via re-assertion of the SYNC signal must not occur for a minimum of four audio frame times following the frame in which the powerdown was triggered. When AC-link powers up the codec indicates readiness via the Codec Ready bit (input slot 0, bit 15).

5.6.2.2. Codec Initiates Wake-up

The STAC9758/59 (running off Vaux) can trigger a wake event (PME#) by transitioning SDATA_IN from low to high and holding it high until either a warm or cold reset is observed on the AC-link. This functionality is typically implemented in modem Codecs that detect ring, Caller ID, etc.

Note that when the AC-link is either programmed to the low power mode or shut off completely, BIT_CLK may stop if the primary codec is supplying the clock, which shuts down the AC-link clock to the Secondary Codec[1]. In order for a Secondary Codec to react to an external event (phone ringing), it must support an independent clocking scheme for any PME# associated logic that must be kept alive when the AC-link is down. This includes logic to asynchronously drive SDATA_IN to a logic high-level which signals a wake request to the AC '97 Digital Controller.

5.6.3. Codec Reset

There are three types of AC '97 reset:

- a *cold* reset where all AC '97 logic (most registers included) is initialized to its default state
- a *warm* reset where the contents of the AC '97 register set are left unaltered
- a *register* reset which only initializes the AC '97 registers to their default states

5.6.4. Cold AC '97 Reset

A cold reset is achieved by asserting RESET# low for the minimum specified time, then subsequently de-asserting RESET# high. BIT_CLK and SDATA_IN will be activated, or re-activated as the case may be, and all AC '97 control registers will be initialized to their default power on reset values.

RESET# is an asynchronous AC '97 input.

5.6.5. Warm AC '97 Reset

A warm AC '97 reset will re-activate the AC-link without altering the current AC '97 register values. A warm reset is signaled by driving SYNC high for a minimum of 1 ms in the absence of BIT_CLK.

Within normal audio frames SYNC is a synchronous AC '97 input. However, in the absence of BIT_CLK, SYNC is treated as an asynchronous input used in the generation of a warm reset to AC '97.

AC '97 MUST NOT respond with the activation of BIT_CLK until SYNC has been sampled low again by AC '97. This will preclude the false detection of a new audio frame.

5.6.6. Register AC '97 Reset

All registers in an AC device can be restored to their default values by performing a write (any value) to the Reset Register, 00h.

1. Secondary Codec always configures its BIT_CLK pin as an input.

6. AC-LINK DIGITAL INTERFACE

6.1. Overview

AC-link is the 5 pin digital serial interface that links AC '97 Codec to Controller. The AC-link protocol is a bi-directional, fixed clock rate, serial digital stream. AC-link handles multiple input and output PCM audio streams, as well as control register accesses employing a time division multiplexed (TDM) scheme that divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution.

The STAC9758/59 DACs, ADCs, and SPDIF can be assigned to slots 3&4, 6&9, 7&8 or 10&11.

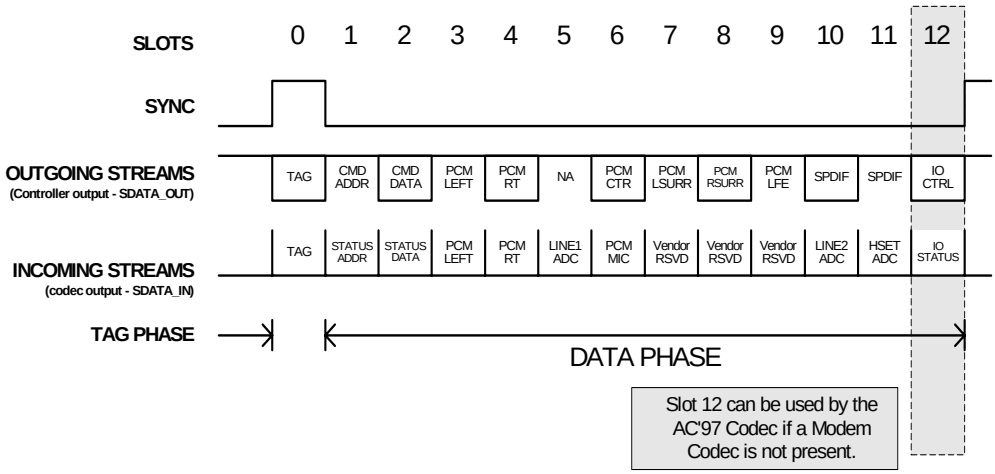


Figure 13. Bi-directional AC-link Frame with Slot assignments

Slot	Name	Description
0	SDATA_OUT TAG	MSBs indicate which slots contain valid data; LSBs convey Codec ID
1	Control CMD ADDR write port	Read/write command bit plus 7-bit Codec register address
2	Control DATA write port	16-bit command register write data
3,4	PCM L&R DAC playback	20-bit PCM data for Left and Right channels
5	Modem Line 1 DAC	16-bit modem data for modem Line 1 output
6,7,8,9	PCM Center, Surround L&R, LFE	20-bit PCM data for Center, Surround L&R, LFE channels
10	4 different uses	A. 20-bit PCM data for SPDIF Left Channel B. extra slots for Double Rate Audio for DAC-A C. extra slots for Double Rate SPDIF C. Modem Line2 DAC
11	4 different uses	A. 20-bit PCM data for SPDIF Right Channel B. extra slots for Double Rate Audio for DAC-A C. extra slots for Double Rate SPDIF D. Modem handset DAC
12	Modem IO control	GPIO write port for modem Control
12	Codec IRQ	Can be used by codec if a modem codec is not present.

Table 4. AC-link output slots (transmitted from the Controller)

Slot	Name	Description
0	SDATA_IN TAG	MSBs indicate which slots contain valid data
1	STATUS ADDR read port	MSBs echo register address; LSBs indicate which slots request data
2	STATUS DATA read port	16-bit command register read data
3,4	PCM L&R ADC record	20-bit PCM data from Left and Right inputs
5	Modem Line 1 ADC	not used by STAC9758/59
6-11	PCM ADC Record	20-bit PCM data - Alternative Slots for Input
12	GPIO Status	GPIO read port and interrupt status

Table 5. The AC-link input slots (transmitted from the Codec)

6.2. AC-link Serial Interface Protocol

The AC '97 Controller signals synchronization of all AC-link data transactions. The AC '97 Codec, Controller, or external clock source drives the serial bit clock onto AC-link, which the AC '97 Controller then qualifies with a synchronization signal to construct audio frames. SYNC, fixed at 48 kHz, is derived by dividing down the serial bit clock (BIT_CLK). BIT_CLK, fixed at 12.288 MHz, provides the necessary clocking granularity to support 12 20-bit outgoing and incoming time slots. AC-link serial data is transitioned on each rising edge of BIT_CLK. The receiver of AC-link data (Codec for outgoing data and Controller for incoming data) samples each serial bit on the falling edges of BIT_CLK.

The AC-link protocol provides for a special 16-bit time slot (Slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A 1 in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream, and contains valid data. If a slot is tagged invalid, it is the responsibility of the source of the data, (AC '97 Codec for the input stream, AC '97 Controller for the output stream), to stuff all bit positions with 0's during that slot's active time.

SYNC remains high for a total duration of 16 BIT_CLKs at the beginning of each audio frame. The portion of the audio frame where SYNC is high is defined as the "Tag Phase". The remainder of the audio frame where SYNC is low is defined as the "Data Phase".

Additionally, for power savings, all clock, sync, and data signals can be halted. This requires that an AC '97 Codec be implemented as a static design to allow its register contents to remain intact when entering a power savings mode.

6.2.1. AC-link Variable Sample Rate Operation

The AC-link serial interconnect defines a digital data and control pipe between the Controller and the Codec. The AC-link supports 12 20-bit slots at 48 kHz on SDATA_IN and SDATA_OUT. The time division multiplexed (TDM) "slot-based" architecture supports a per-slot valid tag infrastructure that the source of each slot's data sets or clears to indicate the validity of the slot data within the current audio frame. This tag infrastructure can be used to support transfers between Controller and Codec at any sample rate.

6.2.2. *Variable Sample Rate Signaling Protocol*

AC-link's tag infrastructure imposes FIFO requirements on both sides of the AC-link. For example, in passing a 44.1 kHz stream across the AC-link, for every 480 audio output frames that are sent across, 441 of them must contain valid sample data. Does the AC '97 Digital Controller pass all 441 PCM samples followed by 39 invalid slots? Or does the AC '97 Digital Controller evenly interleave valid and non-valid slots? Each possible method brings with it different FIFO requirements. To achieve interoperability between AC '97 Digital Controllers and Codecs designed by different manufacturers, it is necessary to standardize the scheme for at least one side of the AC-link so that the FIFO requirements will be common to all designs. The Codec side of the AC-link is the focus of this standardization.

The new standard approach calls for the addition of "on demand" slot request flags. These flags are passed from the Codec to the AC '97 Digital Controller during every audio input frame. Each time the AC '97 Digital Controller sees one or more of the newly-defined slot request flags set active (low) in a given audio input frame, it knows that it must pass along the next PCM sample for the corresponding slot(s) in the AC-link output frame that immediately follows.

The VRA (Variable Rate Audio) bit in the Extended Audio Status and Control Register must be set to 1 to enable variable sample rate audio operation. Setting the VRA=1 has two functions:

1. enables PCM DAC/ADC conversions at variable sample rates by write enabling Sample Rate Registers 2C-34h.
2. enables the on demand Codec-to-Controller signaling protocol using SLOTREQ bits that becomes necessary when a DAC's sample rate varies from the 48 kHz AC-link serial frame rate

The table below summarizes the behavior:

AC '97 functionality	VRA=0	VRA=1
SLOTREQ bits	always 0 (data each frame)	0 or 1 (data on demand)
sample rate registers	forced to 48 kHz	writable

Table 6. VRA Behavior

NOTE: If more than one codec is being used with the SAME controller DMA engine, VRA should NOT be used.

For variable sample rate output, the Codec examines its sample rate control registers, the state of its FIFOs, and the incoming SDATA_OUT tag bits at the beginning of each AC-link output frame to determine which SLOTREQ bits to set active (low). SLOTREQ bits asserted during the current AC-link input frame signal which *active output slots* require data from the AC '97 Digital Controller in the next audio output frame. An *active output slot* is defined as any slot supported by the Codec that is not in a power-down state. For fixed 48 kHz operation the SLOTREQ bits are always set active (low) and a sample is transferred in each frame.

For variable sample rate input, the tag bit for each input slot indicates whether valid data is present or not. Thus, even in variable sample rate mode, the Codec is always the master: for SDATA_IN (Codec to Controller), the Codec sets the TAG bit; for SDATA_OUT (Controller to Codec), the Codec sets the SLOTREQ bit and then checks for the TAG bit in the next frame.

6.2.2.1. SLOTREQ Behavior and Power Management

SLOTREQ bits for fixed rate, powered down, and all unsupported Slots should be driven with 0s for maximum compatibility with the original AC '97 Component Specification. When a DAC channel is powered down, it disappears completely from the serial frame: output tag and slot are ignored, and the SLOTREQ bit is absent (forced to zero).

When the Controller wants to power-down a channel, all it needs to do is:

1. Disable source of DAC samples in Controller
2. Set PR bit for DAC channel in Registers 26h, 2Ah, or 3Eh

When it wants to power up the channel, all it needs to do is:

1. Clear PR bit for DAC channel in Registers 26h, 2Ah, or 3Eh
2. Enable source of DAC samples in Controller

6.2.3. Primary and Secondary Codec Register Addressing

The 2-bit Codec ID field in the LSBs of Output Slot 0 is an addition to the original AC-link protocol that enables an AC ‘97 Digital Controller to independently access Primary and Secondary Codec registers.

For Primary Codec access, the AC ‘97 Digital Controller:

1. Sets the AC-link Frame valid bit (Slot 0, bit 15)
2. *Validates* the tag bits for Slot 1 and 2 Command Address and Data (Slot 0, bits 14 and 13)
3. Sets a *zero* value (00) into the Codec ID field (Slot 0, bits 1 and 0)
4. Transmits the desired Primary Codec Command Address and Command Data in Slots 1 and 2

For Secondary Codec access, the AC ‘97 Digital Controller:

1. Sets the AC-link Frame valid bit (Slot 0, bit 15)
2. *Invalidates* the tag bits for Slot 1 and 2 Command Address and Data (Slot 0, bits 14 and 13)
3. Places a *non-zero* value (01, 10, or 11) into the Codec ID field (Slot 0, bits 1 and 0)
4. Transmits the desired Secondary Codec Command Address and Command Data in Slots 1 and 2

Secondary Codecs disregard the Command Address and Command Data (Slot 0, bits 14 and 13) tag bits unless they see a 2-bit Codec ID value (Slot 0, bits 1 and 0) that matches their configuration. In a sense the Secondary Codec ID field functions as an alternative Valid Command Address (for Secondary reads and writes) and Command Data (for Secondary writes) tag indicator.

Secondary Codecs must monitor the Frame Valid bit, and ignore the frame (regardless of the state of the Secondary Codec ID bits) if it is not valid. AC ‘97 Digital Controllers should set the frame valid bit for a frame with a Secondary register access, even if no other bits in the output tag slot except the Secondary Codec ID bits are set.

6.3. AC-link Output Frame (SDATA_OUT)

The AC-link output frame data streams correspond to the multiplexed bundles of all digital output data targeting AC '97's DAC inputs, and control registers. As mentioned earlier, each AC-link output frame supports up to 12 20-bit outgoing data time slots. Slot 0 is a special reserved time slot containing 16-bits which are used for AC-link protocol infrastructure.

Figure 14 illustrates the time slot based AC-link protocol.

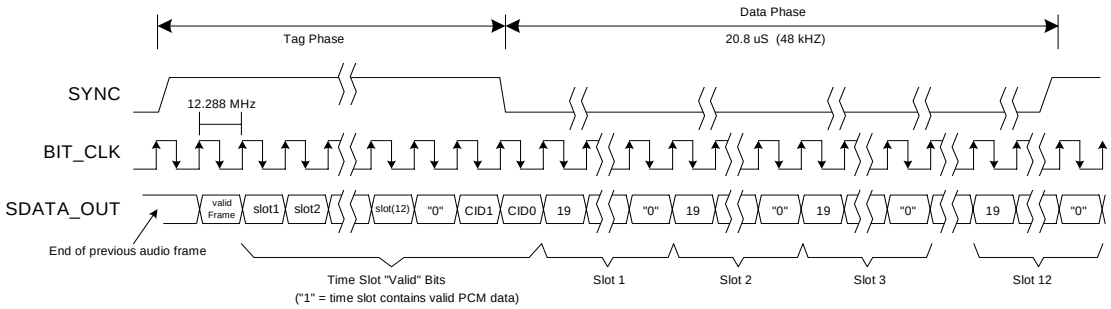


Figure 14. AC-Link Audio Output Frame

A new AC-link output frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the AC '97 Codec samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the AC '97 Controller transitions SDATA_OUT into the first bit position of slot 0 (Valid Frame bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by the AC '97 Codec on the following falling edge of BIT_CLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time aligned.

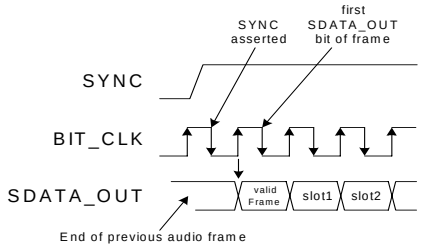


Figure 15. Start of an Audio Output Frame

SDATA_OUT's composite stream is MSB justified (MSB first) with all non-valid slots' bit positions stuffed with 0's by the AC '97 Controller. If there are less than 20 valid bits within an assigned and valid time slot, the AC '97 Controller always stuffs all trailing non-valid bit positions of the 20-bit slot with 0's.

As an example, consider an 8-bit sample stream that is being played out to one of the STAC9758/59 DACs. The first 8-bit positions are presented to the DAC (MSB justified) followed by the next 12 bit-positions which are stuffed with 0's by the AC '97 Controller. This ensures that regardless of the resolution of the implemented DAC (16, 18 or 20-bit), no DC biasing will be introduced by the least significant bits.

When mono audio sample streams are output from the AC '97 Controller it is necessary that BOTH left and right sample stream time slots be filled with the same data.

6.3.1. Slot 0: TAG / Codec ID

Bit	Description
15	Frame Valid
14	Slot 1 Primary Codec Valid Command Address bit (Primary Codec only)
13	Slot 2 Primary Codec Valid Command Data bit (Primary Codec only)
12-3	Slot 3-12 Valid Data bits
12	Slot 3: PCM Left channel
11	Slot 4: PCM Right channel
10	Slot 5: Modem Line 1 (not used on STAC9758/59)
9	Slot 6: Alternative PCM1 Left
8	Slot 7: Alternative PCM2 Left
7	Slot 8: Alternative PCM2 Right
6	Slot 9: Alternative PCM1 Right
5	Slot 10: SPDIF Left
4	Slot 11: SPDIF Right
3	Slot 12: Audio GPIO
2	Reserved (Set to 0)
1-0	2-bit Codec ID field (00 reserved for Primary; 01, 10, 11 indicate Secondary)

Table 7. Output Slot 0 Bit Definitions

NOTE: The DAC can be assigned to slots 3&4, 6&9, 7&8, or 10&11.

Within slot 0 the first bit is a global bit (SDATA_OUT slot 0, bit 15) which flags the validity for the entire audio frame. If the “Valid Frame” bit is a 1, this indicates that the current audio frame contains at least one time slot of valid data. The next 12 bit positions sampled by AC ‘97 indicate which of the corresponding 12 time slots contain valid data. In this way data streams of differing sample rates can be transmitted across AC-link at its fixed 48 kHz audio frame rate.

The two LSBs of Slot 0 transmit the Codec ID used to distinguish Primary and Secondary Codec register access.

6.3.2. Slot 1: Command Address Port

The command port is used to control features, and monitor status (see AC-link input frame Slots 1 and 2) for AC ‘97 Codec functions including, but not limited to, mixer settings, and power management (refer to the control register section of this specification).

The control interface architecture supports up to 64 16-bit read/write registers, addressable on even byte boundaries. Only the even registers (00h, 02h, etc.) are currently defined, odd register (01h, 03h, etc.) accesses are reserved for future expansion.

Note that shadowing of the control register file on the AC ‘97 Controller is an option left open to the implementation of the AC ‘97 Controller. The AC ‘97 Codec’s control register file is nonetheless required to be readable as well as writeable to provide more robust testability.

AC-link output frame slot 1 communicates control register address, and write/read command information to the STAC9758/59.

Bit	Description	Comments
19	Read/Write command	1= read, 0=write
18:12	Control Register Index	sixty-four 16-bit locations, addressed on even byte boundaries
11:0	Reserved	Stuffed with 0's

Table 8. Command Address Port Bit Assignments

The first bit (MSB) sampled by AC '97 indicates whether the current control transaction is a read or a write operation. The following 7 bit positions communicate the targeted control register address. The trailing 12 bit positions within the slot are reserved and must be stuffed with 0's by the AC '97 Controller.

6.3.3. Slot 2: Command Data Port

The command data port is used to deliver 16-bit control register write data in the event that the current command port operation is a write cycle. (as indicated by Slot 1, bit 19)

- Bit(19:4)Control Register Write Data(Stuffed with 0's if current operation is a read)
- Bit(3:0)Reserved (Stuffed with 0's)

If the current command port operation is a read then the entire slot time must be stuffed with 0's by the AC '97 Controller.

6.3.4. Slot 3: PCM Playback Left Channel

AC-link output frame slot 3 is the composite digital audio left playback stream. In a typical 'Games Compatible" PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC '97 Controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the AC '97 Controller must stuff all trailing non-valid bit positions within this time slot with 0's.

The DAC can be assigned to slots 3&4, 6&9, 7&8, or 10&11.

6.3.5. Slot 4: PCM Playback Right Channel

AC-link output frame slot 4 is the composite digital audio right playback stream. In a typical 'Games Compatible" PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC '97 Controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the AC '97 Controller must stuff all trailing non-valid bit positions within this time slot with 0's.

The DAC can be assigned to slots 3&4, 6&9, 7&8, or 10&11.

6.3.6. Slot 5: Modem Line 1 Output Channel

Audio output frame slot 5 is reserved for modem operation and is not used by the STAC9758/59.

6.3.7. Slot 6 -11: DAC

The DAC can be assigned to slots 3&4, 6&9, 7&8, or 10&11.

6.3.8. *Slot 12: Audio GPIO Control Channel*

AC-link output frame slot 12 contains the audio GPIO control outputs.

6.4. AC-link Input Frame (SDATA_IN)

The AC-link input frame data streams correspond to the multiplexed bundles of all digital input data targeting the AC '97 Controller. As is the case for audio output frame, each AC-link input frame consists of 12 20-bit time slots. Slot 0 is a special reserved time slot containing 16-bits which are used for AC-link protocol infrastructure.

The following diagram illustrates the time slot-based AC-link protocol.

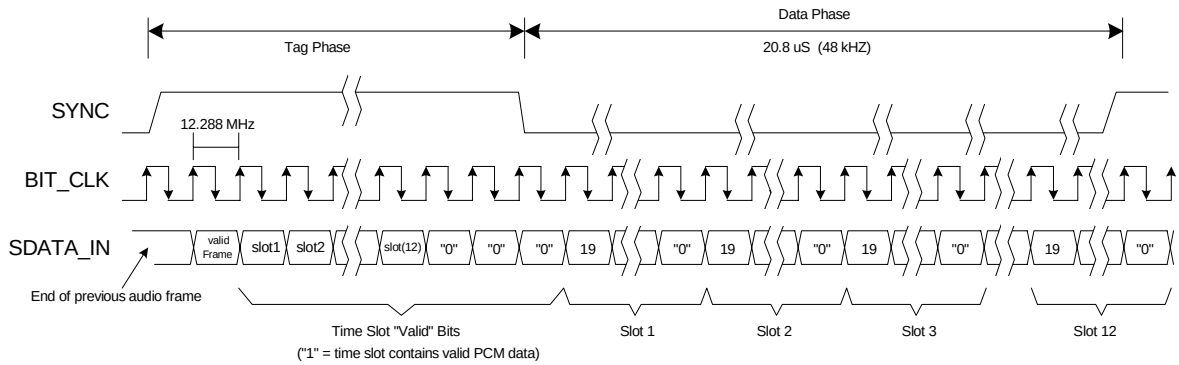


Figure 16. STAC9758/59 Audio Input Frame

A new AC-link input frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the AC '97 Codec samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the AC '97 Codec transitions SDATA_IN into the first bit position of slot 0 ("Codec Ready" bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by the AC '97 Controller on the following falling edge of BIT_CLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time aligned.

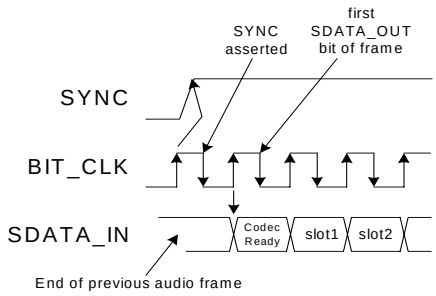


Figure 17. Start of an Audio Input Frame

SDATA_IN's composite stream is MSB justified (MSB first) with all non-valid bit positions (for assigned and/or unassigned time slots) stuffed with 0's by the AC '97 Codec. SDATA_IN data is sampled on the falling edges of BIT_CLK.

6.4.1. Slot 0: TAG

Within slot 0 the first bit is a global bit (SDATA_IN slot 0, bit 15) which flags whether the AC '97 Codec is in the "Codec Ready" state or not. If the "Codec Ready" bit is a 0, this indicates that the AC '97 Codec is not ready for normal operation. This condition is normal following the deassertion of power on reset for example, while the AC '97 Codec's voltage references settle. When the AC-link "Codec Ready" indicator bit is a 1 it indicates that the AC-link and AC '97 Codec control and status registers are in a fully operational state. Codec must assert "Codec Ready" within 400 us after it starts receiving valid SYNC pulses from the controller, to provide indication of connection to the link and Control/Status registers are available for access. The AC`97 Controller and related software **must wait** until all of the lower four bits of the Control/Status Register, 26h, are set before attempting any register writes, or attempting to enable any audio stream, to avoid undesirable audio artifacts.

Prior to any attempts at putting an AC '97 Codec into operation the AC '97 Controller should poll the first bit in the AC-link input frame (SDATA_IN slot 0, bit 15) for an indication that Codec has gone "Codec Ready". Once an AC '97 Codec is sampled "Codec Ready"[1] then the next 12 bit positions sampled by the AC '97 Controller indicate which of the corresponding 12 time slots are assigned to input data streams, and that they contain valid data.

6.4.1.1. Slot 1: Status Address Port / SLOTREQ signaling bits

Bit	Description
19	RESERVED (Set to 0)
18-12	Control Register Index Echo (Set to 0s if tagged "invalid" by AC '97 Codec)
11-2	On Demand Data Request Flags (next output frame): 0= send data 1= do NOT send data
11	Slot 3 request: PCM Left channel
10	Slot 4 request: PCM Right channel
9	Slot 5 request: RESERVED
8	Slot 6 request: PCM Center
7	Slot 7 request: PCM Left Surround
6	Slot 8 request: PCM Right Surround
5	Slot 9 request: PCM LFE
4	Slot 10 request: SPDIF
3	Slot 11 request: SPDIF
2	Slot 12 request: Interrupt Status and GPIO
1,0	RESERVED (Set to 0)

Table 9. Input Slot 1 Bit Definitions

NOTE: The ADC can be assigned to slots 3&4, 6&9, 7&8, or 10&11.

1. There are several subsections within an AC '97 Codec that can independently go busy/ready. It is the responsibility of the AC '97 controller to probe more deeply into the AC '97 Codec's register file to determine which subsections are actually ready (refer to section 6.3 for more information).

6.4.1.2. Status Address Port

The status port is used to monitor status for the STAC9758/59 functions including, but not limited to, mixer settings and power management. AC-link input frame slot 1's stream echoes the control register index, for historical reference, for the data to be returned in slot 2. (Assuming that slots 1 and 2 had been tagged "valid" by the AC '97 Codec during slot 0.

Bit	Description	Comments
19	Reserved	Stuffed with 0's
18:12	Control Register Index	Echo of register index for which data is being returned
11:2	SLOTREQ	See Next Section
1:0	Reserved	Stuffed with 0's

Table 10. Status Address Port Bit Assignments

The first bit (MSB) generated by AC '97 is always stuffed with a 0. The following 7 bit positions communicate the associated control register address, the next 10 bits support AC '97's variable sample rate signaling protocol, and the trailing 2 bit positions are stuffed with 0's by AC '97.

6.4.1.3. SLOTREQ signaling bits

AC-link input frame Slot #1, the Status Address Port, now delivers Codec control register read address *and* variable sample rate slot request flags for all output slots. Ten of the formerly reserved least significant bits have been defined as data request flags for output slots 3-12.

The AC-link input frame Slot 1 tag bit is independent of the bit 11-2 slot request field, and ONLY indicates valid Status Address Port data (Control Register Index). The Codec should only set SDATA_IN tag bits for Slot 1 (Address) and Slot 2 (Data) to 1 when returning valid data from a previous register read. They should otherwise be set to 0. SLOTREQ bits have validity independent of the Slot 1 tag bit.

SLOTREQ bits are always 0 in the following cases

- fixed rate mode (VRA=0)
- inactive (powered down) DAC channel

SLOTREQ bits are only set to 1 by the Codec in the following case

- Variable rate audio mode (VRA=1) AND active (power ready) DAC AND a non-48 kHz DAC sample rate and Codec does not need a sample

6.4.2. Slot 2: Status Data Port

The status data port delivers 16-bit control register read data.

Bit	Description	Comments
19:4	Control Register Read Data	Stuffed with 0's if tagged "invalid"
3:0	Reserved	Stuffed with 0's

Table 11. Status Data Port Bit Assignments

If Slot 2 is tagged invalid by AC '97, then the entire slot will be stuffed with 0's by AC '97.

6.4.3. Slot 3: PCM Record Left Channel

Audio input frame slot 3 is the left channel output of STAC9758/59 input MUX, post-ADC. STAC9758/59 ADCs are implemented to support 20-bit resolution.

The ADC can be assigned to slots 3&4, 6&9, 7&8, or 10&11.

SPDIF_IN can be assigned to slots 3&4, 6&9, 7&8, or 10&11.

6.4.4. Slot 4: PCM Record Right Channel

Audio input frame slot 4 is the right channel output of STAC9758/59 input MUX, post-ADC. STAC9758/59 ADCs are implemented to support 20-bit resolution.

The ADC can be assigned to slots 3&4, 6&9, 7&8, or 10&11.

SPDIF_IN can be assigned to slots 3&4, 6&9, 7&8, or 10&11.

6.4.5. Slot 5: Modem Line 1 ADC

Audio input frame slot 5 is not used by the STAC9758/59 and are always stuffed with 0's.

6.4.6. Slot 6-9: ADC

The left and right ADC channels of the STAC9758/59 may be assigned to slots 6&9 by Register 6Eh.

The ADC can be assigned to slots 3&4, 6&9, 7&8, or 10&11.

SPDIF_IN can be assigned to slots 3&4, 6&9, 7&8, or 10&11.

6.4.7. Slots 7-8: Vendor Reserved

The left and right ADC channels of the STAC9758/59 may be assigned to slots 7&8 by Register 6Eh.

The ADC can be assigned to slots 3&4, 6&9, 7&8, or 10&11.

SPDIF_IN can be assigned to slots 3&4, 6&9, 7&8, or 10&11.

6.4.8. Slot 10 & 11: ADC

The left and right ADC channels of the STAC9758/59 may be assigned to slots 10&11 by Register 6Eh.

The ADC can be assigned to slots 3&4, 6&9, 7&8, or 10&11.

SPDIF_IN can be assigned to slots 3&4, 6&9, 7&8, or 10&11.

6.4.9. Slot 12: Reserved

AC-link input frame slot 12 contains the GPIO status inputs and allows for audio interrupts. Slot 12 can be used by the AC'97 codec if a modem codec is not present.

6.5. AC-link Interoperability Requirements and Recommendations

6.5.1. "Atomic slot" Treatment of Slot 1 Address and Slot 2 Data

Command or Status Address and Data cannot be split across multiple AC-link frames. The following transactions require that valid Slot 1 Address and valid Slot 2 Data be treated as "atomic" (inseparable) with Slot 0 Tag bits for Address and Data set accordingly (that is, both valid):

1. AC '97 Digital Controller write commands to Primary Codecs
2. AC '97 Codec status responses

Whenever the AC '97 Digital Controller addresses a Primary Codec or an AC '97 Codec responds to a read command, Slot 0 Tag bits should always be set to indicate actual Slot 1 and Slot 2 data validity.

Function	Slot 0, bit 15 (Valid Frame)	Slot 0, bit 14 (Valid Slot 1 Address)	Slot 0, bit 13 (Valid Slot 2 Data)	Slot 0, Bits 1-0 (Codec ID)
AC '97 Digital Controller Primary Read Frame N, SDATA_OUT	1	1	0	00
AC '97 Digital Controller Primary WriteFrame N, SDATA_OUT	1	1	1	00
AC '97 Codec Status Frame N+1, SDATA_IN	1	1	1	00

Table 12. Primary Codec Addressing: Slot 0 Tag Bits

When the AC '97 Digital Controller addresses a Secondary Codec, the Slot 0 Tag bits for Address and Data must be 0. A non-zero, 2-bit Codec ID in the LSBs of Slot 0 indicates a valid Read or Write Address in Slot 1, and the Slot 1 R/W bit indicates presence or absence of valid Data in Slot 2.

6.6. Slot Assignments for Audio

Function	Slot 0, bit 15 (Valid Frame)	Slot 0, bit 14 (Valid Slot 1 Address)	Slot 0, bit 13 (Valid Slot 2 Data)	Slot 0, Bits 1-0 (Codec ID)
AC '97 Digital Controller Secondary Read Frame N, SDATA_OUT	1	0	0	01, 10, or 11
AC '97 Digital Controller Secondary Write Frame N, SDATA_OUT	1	0	0	01, 10, or 11
AC '97 Codec Status Frame N+1, SDATA_IN	1	1	1	00

Table 13. Secondary Codec Addressing: Slot 0 tag bits

NOTE: The DAC & ADC can be assigned to slots 3&4, 6&9, 7&8, or 10&11.

The AC-link output slots dedicated to audio are defined as follows:

Slot	ADAT Channel	Name	Description
3	0	Slot Pair 1L	20-bit PCM data, typically Front Left Channel
4	1	Slot Pair 1R	20-bit PCM data, typically Front Right Channel
5	n/a	Not Used	Not used
6	4	Slot Pair 3L	20-bit PCM data, typically Center Channel
7	2	Slot Pair 2L	20-bit PCM data, typically Rear Left Channel

Table 14. ACLink Slot Definitions

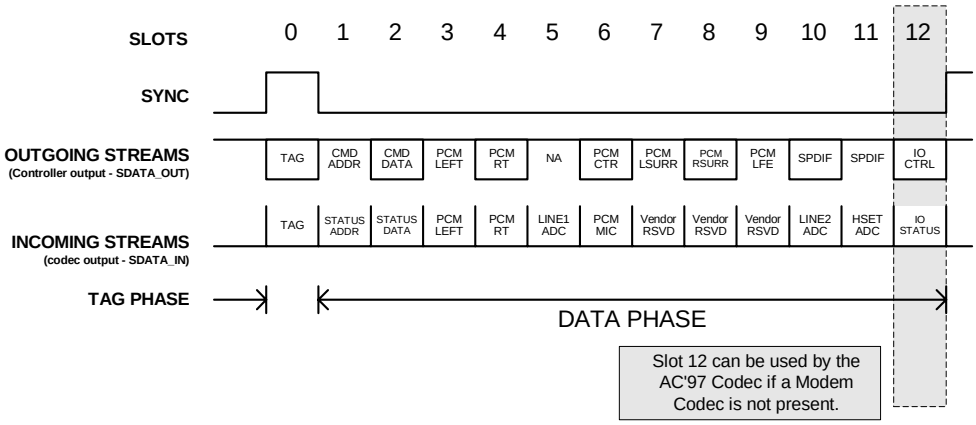


Figure 18. Bi-directional AC-link Frame with Slot assignments

Slot	ADAT Channel	Name	Description
8	3	Slot Pair 2R	20-bit PCM data, typically Rear Right Channel
9	5	Slot Pair 3R	20-bit PCM data, typically LFE Channel
10	6	Slot Pair 4L	20-bit PCM data, typically SPDIF Left Channel
11	7	Slot Pair 4R	20-bit PCM data, typically SPDIF Right Channel
12	n/a	Interrupt Control	Provides optional interrupt capability for Audio Codec (not usable when a modem is present)

Table 14. ACLink Slot Definitions (Continued)

The AC-link input slots dedicated to audio are defined as follows:

Slot	Name	Description
3	Slot Pair 1L	20-bit PCM incoming data from Left Channel
4	Slot Pair 1R	20-bit PCM incoming data from Right Channel
5	Not used	Not used
6	Slot Pair 3L	20-bit PCM incoming data from Left Channel
7	Slot Pair 2L	20-bit PCM incoming data from Right Channel
8	Slot Pair 2R	20-bit PCM incoming data from Left Channel
9	Slot Pair 3R	20-bit PCM incoming data from Right Channel
10	Slot Pair 4L	20-bit PCM incoming data from Left Channel
11	Slot Pair 4R	20-bit PCM incoming data from Right Channel
12	Interrupt Control	Provides optional interrupt capability for Audio Codec (not usable when a modem is present)

Table 15. AC-link input slots dedicated to audio

The ADC and the SPDIF Inputs can be separately assigned to any of the four slot pairs. However, they cannot both be assigned to the same slot pair.

Bit	Description
19-1	Reserved (STAC9758/59 will return zeros in bits 19-1)
0	Assertion = 1 will cause interrupt to be propagated to Audio controller system interrupt. See register 24h definition for enabling mechanism.

Table 16. Audio Interrupt Slot Definitions

7. STAC9758/59 MIXER

- Mixer Inputs
  - Analog PC Beep, Digital PC Beep, Phone, Aux In, Line In (has pre-select mux for jack sharing/Universal Jacks™), Mic In (mono and stereo modes - includes pre-select mux), DAC-A, DAC-B
  - Split-mute option on all stereo inputs allows left and right inputs to be muted independently.
- Analog Output Sources
  - DAC-A, DAC-B, DAC-C, Stereo Mix, Mono
- Analog I/O
  - Pins 21/22, 23/24, 35/36, 39/41, 43/44
  - All Analog I/O pins have analog jack sense
  - Pins 35/36 and 39/41 are capable of driving headphones
  - All outputs are tri-stated when powered down
- Split-mute (bit D7) option on all outputs allows left and right outputs to be muted independently.

7.1. SPDIF Digital Mux

The STAC9758/59 incorporates a digital output that supports SPDIF formats. A multiplexer determines which of two digital input streams are used for the digital output conversion process. These two streams include the PCM OUT data from the audio controller and the ADC recorded output. The normal analog LINE_OUT signal can be converted to the SPDIF formats by using the internal ADC to record the ‘MIX” output, which is the combination of all analog and all digital sources. In the case of digital controllers with support for 4 or more channels, the SPDIF output mode can be used to support compressed 6-channel output streams for delivery to home theater systems. These can be routed on alternate AC-Link slots to the SPDIF output, while the standard 2-channel output is delivered as selected by bits D5 and D4 in Register 6E. If the digital controller supports 6 channels, a SPDIF output with 4 analog channels can also be configured.

If the Digital Controller has independent DMA engines, SPDIF and Analog can be used simultaneously and independently.

7.2. SPDIF_IN

The STAC9758 implements a multi-function pin in place of the traditional EAPD pin (pin 47.) EAPD functionality is supported as the default for compatibility with existing software. Advanced implementations can utilize this pin as an alternate GPIO or SPDIF_IN.

A sophisticated digital PLL allows automatic rate detection and accurate data recovery. The ability to accept consumer SPDIF voltage levels directly eliminates the need for costly external receiver ICs. Advanced features such as record slot select and SPDIF_IN routing to the surround DACs allows simultaneous record and playback as well as multi-channel recording.

7.3. ADAT Optical "Lightpipe" Support

Pin 48 can be switched to an alternate ADAT Optical Output mode to provide up to 8 channels of royalty-free uncompressed 24-bit, 48 kHz and 44.1 kHz digital audio. An ADAT Optical receiver is required to decode the data. This mode of operation is only intended for use with optical connections.

7.4. Digital PC Beep

The STAC9758/59 offers 2 styles of PC Beep, Digital and Analog. The digital PC Beep is a new feature required by AC'97 2.3. This style of PC Beep will eventually replace the Analog style, thus eliminating the need for a PC Beep pin. Until this feature is widely accepted, all SigmaTel AC97 2.3 codecs will provide both styles of PC Beep. Both PC Beep styles use Reg 0Ah. Additional information about Register 0Ah can be found in Section 9.0.5: page 50.

7.5. Double Rate Audio

DAC-A (Front) can be operated at double the normal Sample Rate. If the DRA Enable bit (Reg 2A, Bit D1) is set, DAC-A will make use of an extra slot pair to provide twice the normal amount of data passed through AC-Link, thus providing two samples per frame instead of one. Slot pair 3/4 must be used for the primary slot pair. The secondary slot pair is defined by the DRSS bits (Reg 20, Bits D11:D10).

If VRA = 0 and DRA = 1, then the output sample rate is fixed at 96 kHz. If VRA = 1 and DRA = 1, then the output is double the rate specified in PCM DAC Rate, Reg 2Ch.

7.6. Double Rate SPDIF Output

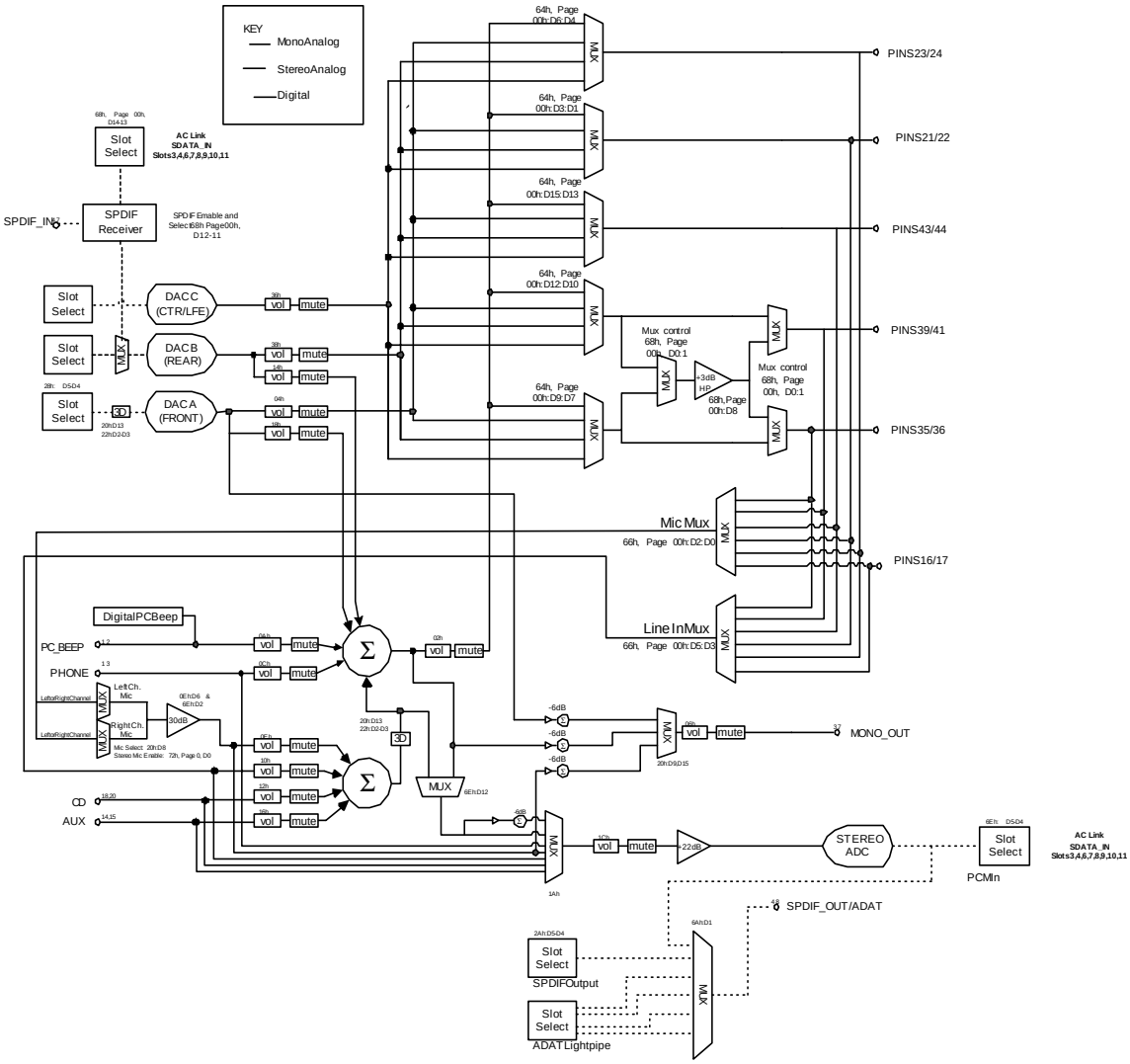
SPDIF Output can run at 96 kHz. If the DRA Enable bit (Reg 2A, Bit D1) is set, the SPDIF Output will make use of an extra slot pair to provide twice the normal amount of data passed through AC-Link, thus providing two samples per frame instead of one. Slot pair 3/4 must be used for the primary slot pair. The secondary slot pair is defined by the SPSA bits (Reg 2A, Bits D4:D5).

Double Rate support for ADAT Output is not present. ADAT Output sample rates are limited to 48 kHz and 44.1 kHz.

To simultaneously use Double-Rate Audio and Double-Rate SPDIF Output, the Controller or Driver must set DRSS and SPSA bits to refer to the same set of secondary slots. The primary slot pair for either output will automatically be selected as 3&4 when the DRA and DRS bits are set.

Also, the Controller or Driver should make sure that PCM DAC Rate (Reg 2Ch) and SPSR are set to equivalent values, since the slots are being shared.

8. STAC9758/59 MIXER DIAGRAM



9. PROGRAMMING REGISTERS

Address	Name	Default	Location
00h	Reset	6A90h	9.0.1; page 47
02h	Master Volume	8000h	9.0.2; page 48
04h	DAC-A Volume	8000h	9.0.3; page 49
06h	Master Volume MONO	8000h	9.0.4; page 50
0Ah	PC Beep Volume	0000h	9.0.5; page 50
0Ch	Phone Volume	8008h	9.0.7; page 51
0Eh	Mono/Stereo Mic Volume	8008h	9.0.8; page 52
10h	Line In Volume	8808h	9.0.8.2; page 53
12h	CD Volume	8808h	9.0.10; page 55
14h	DAC-B to Mixer2 Volume	8808h	9.0.11; page 56
16h	Aux Mixer Volume	8808h	9.0.13; page 58
18h	PCM Out Mixer Volume	8808h	9.0.14; page 59
1Ah	Record Select	0000h	9.0.15; page 60
1Ch	Record Gain	8000h	9.0.16; page 61
20h	General Purpose	0000h	9.0.17; page 62
22h	3D Control	0000h	9.0.18; page 63
24h	Audio Int. & Paging	0000h	9.0.19: page 64
26h	Powerdown Ctrl/Stat	000Fh	9.0.20; page 65
28h	Extended Audio ID	0BC7h	9.0.21; page 66
2Ah	Extended Audio Control/Status	05F0h	9.0.22; page 68
2Ch	PCM DAC Rate (DAC-A & DAC-CL)	BB80h	9.0.24; page 71
2Eh	PCM Surr DAC Rate (DAC-B)	BB80h	9.0.25; page 71
30h	PCM LFE DAC Rate (DAC-CR)	BB80h	9.0.26; page 72
32h	PCM LR ADC Rate	BB80h	9.0.27; page 72
36h	Center/LFE Volume	8080h	9.0.28; page 72
38h	Surround Volume	8080h	9.0.29; page 73
3Ah	SPDIF Control	2000h	9.0.30; page 74
3Eh	Extended Modem Stat/Ctl	0100h	9.1.4; page 76
4Ch	GPIO Pin Configuration	000Fh	9.1.5; page 76
4Eh	GPIO Pin Polarity/Type	FFFFh	9.1.6; page 77
50h	GPIO Pin Sticky	0000h	9.1.7; page 77
52h	GPIO Pin Mask	0000h	9.1.8; page 78
54h	GPIO Pin Status	0000h	9.1.9; page 78
60h	SPDIF In Status 1	0000h	9.3.1; page 80
60h (Page 01h)	Codec Class/Rev	18xxh	9.3.2; page 80

Table 17. Programming Registers

Address	Name	Default	Location
62h	SPDIF IN Status 2	0000h	9.3.3; page 81
62h (Page 01h)	PCI SVID	FFFFh	9.3.4; page 82
64h	Universal Jacks™ Output Select	D794h	9.3.3; page 81
64h (Page 01h)	PCI SSID	FFFFh	9.3.6; page 83
66h	Universal Jacks™ Input Select	0000h	9.3.5: page 82
66h (Page 01h)	Function Select	0000h	9.3.8; page 85
68h	I/O Misc.	0000h	9.3.7: page 84
68h (Page 01h)	Function Information	0010h	9.3.10; page 87
6Ah	Digital Audio Control	0000h	9.3.9; page 86
6Ah (Page01h)	Sense Details	N/A	9.3.12: page 90
6Ch	Revision Code	xxxxh	9.3.12; page 90
6Ch (Page01h)	DAC Slot Mapping	3760h	9.3.14; page 91
6Eh	Analog Special	1000h	9.3.14: page 91
6Eh (Page01h)	ADC Slot Mapping	3000h	9.3.16; page 94
70h	SigmaTel Reserved	0000h	9.3.17: page 94
72h	Various Functions	0000h	9.3.19: page 96
74h	EAPD Access	0800h	9.3.19: page 96
76h	Analog Misc.	0000h	9.3.20: page 97
78h	ADAT Control and HPF Bypass	0000h	9.3.21: page 97
7Ah	SigmaTel Reserved	0000h	9.3.22: page 97
7Ch	Vendor ID1	8384h	9.4.1; page 98
7Eh	Vendor ID2	7658h	9.4.2; page 98

Table 17. Programming Registers (Continued)

9.0.1. Reset (00h)

Default: 6A90h

D15	D14	D13	D12	D11	D10	D9	D8
RSRVD	SE4	SE3	SE2	SE1	SE0	ID9	ID8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Writing any value to this register performs a register reset, which causes most** registers to revert to their default values. This register reset also resets all the digital block. Reading this register returns information about the part.

Bit(s)	Reset Value	R/W	Name	Description
15	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
14:10	11010	RO	SE4:SE0	SIGMATEL ID for SS3D
9	1	RO	ID9	20 BIT ADC RESOLUTION (supported)
8	0	RO	ID8	18 BIT ADC RESOLUTION
7	1	RO	ID7	20 BIT DAC RESOLUTION (supported)
6	0	RO	ID6	18 BIT DAC RESOLUTION
5	0	RO	ID5	LOUDNESS/BASS BOOST (not supported)
4	1	RO	ID4	HEADPHONE OUT (supported)
3	0	RO	ID3	SIMULATED STEREO (not supported))
2	0	RO	ID2	BASS & TREBLE CONTROL (not supported)
1	0	RO	ID1	RESERVED
0	0	RO	ID0	Dedicated MIC PCM IN CHANNEL (not supported)

9.0.2. Master Volume Registers (02h)

Controls Volume of Stereo Mix Output.

Default: 8000h

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED	ML5	ML4	ML3	ML2	ML1	ML0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RMute	RESERVED	MR5	MR4	MR3	MR2	MR1	MR0

Bit(s)	Reset Value	R/W	Name	Description
15	1	RW	Mute	0 = no mute 1 = mute The channels to be affected are determined by the SPLITMUTE bit (Reg 72, Page 0, Bit D6) If SPLITMUTE = 0 - both Left and Right channels are muted If SPLITMUTE = 1 - only the Left Channel is muted
14	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
13	0	WO	ML5	If a 1 is written to this bit, then ML<4:0> is loaded with 11111b. This bit always reads 0.
12:8	0	RW	ML<4:0>	Left Lineout Volume Control 00h = 00000b = 0 dB attenuation 01h = 00001b = -1.5 dB attenuation ..... 1Fh = 11111b = -46.5 dB attenuation
7	0	RW	RMute	Mutes Right Channel independent of Left Channel 0=no mute 1=mute The SPLITMUTE bit (Reg 72,Page 0, Bit D6) must be set to 1 in order for the RMute bit to have an effect. The RMute bit is R/W, and may be written and read regardless of the state of the SPLITMUTE bit.
6	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
5	0	WO	MR5	If a 1 is written to this bit, then MR<4:0> is loaded with 11111b. This bit always reads 0.
4:0	0	RW	MR<4:0>	Right Channel Lineout Volume Control 00h = 00000b = 0 dB attenuation 01h = 00001b = -1.5 dB attenuation ..... 1Fh = 11111b = -46.5 dB attenuation

9.0.3. DAC-A Volume Register (04h)

Default: 8000h

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED	ML5	ML4	ML3	ML2	ML1	ML0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RMute	RESERVED	MR5	MR4	MR3	MR2	MR1	MR0

Bit(s)	Reset Value	R/W	Name	Description
15	1	RW	Mute	0 = no mute 1 = mute The channels to be affected are determined by the SPLITMUTE bit (Reg 72, Page 0, Bit D6) If SPLITMUTE = 0 - both Left and Right channels are muted If SPLITMUTE = 1 - only the Left Channel is muted
14	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
13	0	WO	ML5	If a 1 is written to this bit, then ML<4:0> is loaded with 11111b. This bit always reads 0.
12:8	0	RW	ML<4:0>	DAC A Left Volume Control 00h = 00000b = 0 dB attenuation 01h = 00001b = -1.5 dB attenuation ..... 1Fh = 11111b = -46.5 dB attenuation
7	0	RW	RMute	Mutes Right Channel independent of Left Channel 0=unmute 1=muted The SPLITMUTE bit (Reg 72 (Page 0), D6) must be set to 1 in order for the RMute bit to have an effect on the sound. The RMute bit is R/W. The RMute bit may be written and read regardless of the state of the SPLITMUTE bit.
6	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
5	0	WO	MR5	If a 1 is written to this bit, then MR<4:0> is loaded with 11111b. This bit always reads 0.
4:0	0	RW	MR<4:0>	DAC A Right Volume Control 00h = 00000b = 0 dB attenuation 01h = 00001b = -1.5 dB attenuation ..... 1Fh = 11111b = -46.5 dB attenuation

9.0.4. Master Volume MONO (06h)

Default: 8000h

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED						
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED		MM5	MM4	MM3	MM2	MM1	MM0

Bit(s)	Reset Value	R/W	Name	Description
15	1	RW	Mute	0=no mute 1=mute MONO output
14:6	0	RO	RESERVED	BITS NOT USED, SHOULD READ BACK 0
5	0	WO	MM5	If a 1 is written to this bit, then MM<4:0> is loaded with 11111b. This bit always reads 0.
4:0	0	RW	MM<4:0>	Mono Volume Control 00h = 00000b = 0 dB attenuation 01h = 00001b = -1.5 dB attenuation ..... 1Fh = 11111b = -46.5 dB attenuation

9.0.5. PC BEEP Volume (0Ah)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED	PC_BEEP_FD	F7	F6	F5	F4	F3
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
F2	F1	F0	PV3	PV2	PV1	PV0	RSRVD

Bit(s)	Reset Value	R/W	Name	Description
15	0	RW	Mute	0=no mute 1=mute pc beep signal
14	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
13	0	RO	PC_BEEP_FD	PC BEEP Frequency Divide
12:5	00h	RW	F[7:0]	The Beep frequency is the result of dividing the 48KHz clock by 4 times the number specified in F[7:0] allowing tones from 47Hz to 12KHz. A value of 00h in bits F[7:0] disables internal PC BEEP generation and enables external PC BEEP input if available.
12:5	00h	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
4:1	0	RW	PV(3:0)	PCBEEP Volume Control 00h = 0000b = 0 dB attenuation 00h = 0001b = -3 dB attenuation ..... 0Fh = 1111b = -45 dB attenuation
0	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0

9.0.6. Digital PC Beep

The AC97 2.3 specification calls for the codec to generate a square wave tone at a particular volume and frequency. Typically, the BIOS will program this register during the Power On Self Test (POST) cycle.

To use create a tone using Digital PC Beep, write a non-zero value to the F Bits in Reg 0Ah (bits D12:D5). The beep frequency is the result of dividing the 48KHz clock by 4 times the number specified in F[7:0], allowing tones from 47Hz to 12KHz. (see Table 18: page 51). Set the PV bits in Reg 0Ah, (Bits D4:D1) control the volume level from 0 to 45dB of attenuation in 3dB steps. Unmute bit D15 if necessary.

To stop the tone, write 801Fh to Reg 0Ah. This turns off the generator, turns the volume to the lowest setting, and mutes the register.

Applying a signal to the PC Beep pin, pin 12, may cause the digital PC Beep signal to become distorted or inaudible. When using the digital PC Beep feature, it is recommended to leave the PC Beep input pin connected to analog ground through a capacitor. Connecting a capacitor from the PC Beep input pin to ground will create a more pleasing sound by changing the digital output to a more sinusoidal like output.

Value	Reg 0Ah	Frequency
1	0x01	12,000Hz
10	0x0A	1200Hz
25	0x19	480Hz
50	0x32	240Hz
100	0x64	120Hz
127	0x0F	94.48Hz
255	0xFF	47.05Hz

Table 18. Digital PC Beep Examples

Typically this feature will be used exclusively by the BIOS, and will not be used by Controller or Driver.

9.0.7. Phone Volume (0Ch)

Default: 8008h.

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED						
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED			GN4	GN3	GN2	GN1	GN0

Bit(s)	Reset Value	R/W	Name	Description
15	1	RW	Mute	0=no mute 1=mute phone
14:5	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
4:0	08	RW	GN<4:0>	Phone Volume Control 00h = 00000b = +12.0 dB gain 01h = 00001b = +10.5 dB gain ..... 08h = 01000b = 0.0 dB - unity gain (default) ..... 1Fh = 11111b = -34.5 dB attenuation

9.0.8. Mono/Stereo Mic Volume (0Eh)

Mic is actually one of 6 possible stereo input sources selected by the MicMux (Reg 66h, Page 0, Bits D2:D0). Each of these sources may be selected as mono Left, mono Right, stereo, or stereo L-R swapped. Boosts of 10, 20, or 30dB are available to all inputs controlled by the mic mux.

9.0.8.1. Mic Volume Register in Mono Mode (default mode for Reg 0Eh)

Enabled when Stereo Mic Enable Bit (STMICEN), Reg 72h, Page 0, Bit D0 = 0

Default: 8008h.

D15	D14	D13	D12	D11	D10	D9	D8
ALLMute	RESERVED						
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED	BOOSTEN	RESERVED	GN4	GN3	GN2	GN1	GN0

Bit(s)	Reset Value	R/W	Name	Description
15	1	RW	ALLMute	Mutes Left and Right Channel Mic 0=no mute 1=muted
14:8	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
7	0	RW	RMute	Mutes Right Channel independent of Left Channel 0=unmute 1=muted The SPLITMUTE bit (Reg 72, Page 0, Bit D6) and STMICEN bit (Reg 72, Page 0, Bit D0) must both be set to 1's in order for the RMute bit to have an effect on the sound. The RMute bit is R/W. The RMute bit may be written and read regardless of the state of the SPLITMUTE and STMICEN bits.
6	0	RW	BOOSTEN	Works with MICGAINVAL (Register 6Eh, Bit D2) BOOSTEN MICGAINVAL 0 0 = 0 dB 0 1 = 10 dB 1 0 = 20 dB 1 1 = 30 dB
5	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
4:0	08	RW	GN<4:0>	Mic Volume Control 00h = 00000b = +12.0 dB gain 01h = 00001b = +10.5 dB gain ..... 08h = 01000b = 0.0 dB - unity gain (default) ..... 1Fh = 11111b = -34.5 dB attenuation

9.0.8.2. Mic Volume Register in Stereo Mode (Reg 0Eh)

Enabled when Stereo Mic Enable Bit (STMICEN), Reg 72h, Page 0, Bit D0 = 1

Default: 8008h.

D15	D14	D13	D12	D11	D10	D9	D8
LMute	RESERVED		GNL4	GNL3	GNL2	GNL1	GNL0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RMute	BOOSTEN	RESERVED	GNR4	GN3	GNR2	GNR1	GNR0

Bit(s)	Reset Value	R/W	Name	Description
15	1	RW	LMute	0 = no mute 1 = mute The channels to be affected are determined by the SPLITMUTE bit (Reg 72, Page 0, D6) If SPLITMUTE = 0 both Left and Right channels are muted If SPLITMUTE = 1 only the Left Channel is muted
14:13	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
12:8	0	RW	GNL<4:0>	STEREO Mic Left Volume Control 00h = 00000b = +12.0 dB gain 01h = 00001b = +10.5 dB gain ..... 08h = 01000b = 0 dB - unity gain ..... 1Fh = 11111b = -34.5 dB attenuation
7	0	RW	RMute	Mutes Right Channel independent of Left Channel 0=unmute 1=muted The SPLITMUTE bit (Reg 72, Page 0, Bit D6) must be set to 1 in order for the RMute bit to have an effect on the sound. The RMute bit is R/W. The RMute bit may be written and read regardless of the state of the SPLITMUTE bit.
6	0	RW	BOOSTEN	Turns on 20 dB of boost in the Microphone Preamp Works in conjunction with MICGAINVAL (Register 6Eh, Page 0, Bit D2) which provides a 10 dB boost in the Microphone preamp. BOOSTEN MICGAINVAL 0 0 = 0 dB 0 1 = 10 dB 1 0 = 20 dB 1 1 = 30 dB
5	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
4:0	0	RW	GNR<4:0>	STEREO Mic Right Channel Volume Control 00h = 00000b = +12.0 dB gain 01h = 00001b = +10.5 dB gain ..... 08h = 01000b = 0 dB - unity gain ..... 1Fh = 11111b = -34.5 dB attenuation

9.0.9. Line In Volume (10h)

Default: 8808h.

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED		GL4	GL3	GL2	GL1	GR0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RMute	RESERVED		GR4	GR3	GR2	GR1	GR0

Bit(s)	Reset Value	R/W	Name	Description
15	1	RW	Mute	0 = no mute 1 = mute The channels to be affected are determined by the SPLITMUTE bit (Reg 72, Page 0, D6) If SPLITMUTE = 0 - both Left and Right channels are muted If SPLITMUTE = 1 - only the Left Channel is muted
14:13	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
12:8	08	RW	GL<4:0>	Left LineIn Volume Control for Stereo Mix 00h = 00000b = +12.0 dB gain 01h = 00001b = +10.5 dB gain ..... 08h = 01000b = 0 dB - unity gain (default) ..... 1Fh = 11111b = -34.5 dB attenuation
7	0	RW	RMute	Mutes Right Channel independent of Left Channel 0=unmute 1=muted The SPLITMUTE bit (Reg 72 (Page 0), D6) must be set to 1 in order for the RMute bit to have an effect on the sound. The RMute bit is R/W. The RMute bit may be written and read regardless of the state of the SPLITMUTE bit.
6:5	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
4:0	08	RW	GR<4:0>	Right LineIn Volume Control for Stereo Mix 00h = 00000b = +12.0 dB gain 01h = 00001b = +10.5 dB gain ..... 08h = 01000b = 0 dB - unity gain (default) ..... 1Fh = 11111b = -34.5 dB attenuation

Line_In may be assigned to one of 6 different pairs of input pins. See Register 66h, Page 0, for more info.

9.0.10. CD Volume (12h)

Default: 8808h.

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED		GL4	GL3	GL2	GL1	GR0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RMute	RESERVED		GR4	GR3	GR2	GR1	GR0

Bit(s)	Reset Value	R/W	Name	Description
15	1	RW	Mute	0 = no mute 1 = mute The channels to be affected are determined by the SPLITMUTE bit (Reg 72, Page 0, D6) If SPLITMUTE = 0 - both Left and Right channels are muted If SPLITMUTE = 1 - only the Left Channel is muted
14:13	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
12:8	08	RW	GL<4:0>	Left CD Volume Control 00h = 00000b = +12.0 dB gain 01h = 00001b = +10.5 dB gain ..... 08h = 01000b = 0 dB - unity gain (default) ..... 1Fh = 11111b = -34.5 dB attenuation
7	0	RW	RMute	Mutes Right Channel independent of Left Channel 0=unmute 1=muted The SPLITMUTE bit (Reg 72 (Page 0), D6) must be set to 1 in order for the RMute bit to have an effect on the sound. The RMute bit is R/W. The RMute bit may be written and read regardless of the state of the SPLITMUTE bit.
6:5	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
4:0	08	RW	GR<4:0>	Right CD Volume Control 00h = 00000b = +12.0 dB gain 01h = 00001b = +10.5 dB gain ..... 08h = 01000b = 0 dB - unity gain (default) ..... 1Fh = 11111b = -34.5 dB attenuation

9.0.11. DAC-B to Mixer2 Volume Control (14h)

Default: 8808h.

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED		GL4	GL3	GL2	GL1	GR0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RMute	RESERVED		GR4	GR3	GR2	GR1	GR0

Bit(s)	Reset Value	R/W	Name	Description
15	1	RW	Mute	0 = no mute 1 = mute The channels to be affected are determined by the SPLITMUTE bit (Reg 72, Page 0, D6) If SPLITMUTE = 0 both Left and Right channels are muted If SPLITMUTE = 1 only the Left Channel is muted
14:13	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
12:8	08	RW	GL<4:0>	DAC-BL Volume Control 00h = 00000b = +12.0 dB gain 01h = 00001b = +10.5 dB gain ..... 08h = 01000b = 0 dB - unity gain (default) ..... 1Fh = 11111b = -34.5 dB attenuation
7	0	RW	RMute	Mutes Right Channel independent of Left Channel 0=unmute 1=muted The SPLITMUTE bit (Reg 72 (Page 0), D6) must be set to 1 in order for the RMute bit to have an effect on the sound. The RMute bit is R/W. The RMute bit may be written and read regardless of the state of the SPLITMUTE bit.
6:5	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
4:0	08	RW	GR<4:0>	DAC-BR Volume Control 00h = 00000b = +12.0 dB gain 01h = 00001b = +10.5 dB gain ..... 08h = 01000b = 0 dB - unity gain (default) ..... 1Fh = 11111b = -34.5 dB attenuation

9.0.12. Video In Use

The STAC9758 Video In path to the mixer including the volume control of Register 14h is used by DAC-B. The Video In pins been redefined as the second microphone input. However, the ***Video Input functionality can be implemented by the flexible input/output structure of the STAC9758, called Universal Jacks.*** This technology allows for selectable input paths. The STAC9758 has a Line In Mux that can select a variety of input options. Using the Line In Mux to select pin 16 and 17, this will set up an extra Line In that can be used as Video In. Line In will still be available using the standard pins 23 and 24, and its volume will be controlled by Register 02h.

- "Use the same pins for Video (pins 16 and 17)
- "Use the Universal Jack Input Select Register (66h), bits D10:8 = 000b to select Line In on Pin 16/17
- "Volume will be controlled by Register 10h (as Video is acting as Line In)
- "The Line In slider now will control Video.
- "Recording is done by using the Line In Record function in the Record Select Register (1Ah), by setting the left and/or right channel input select to Line In
    - Left Line In Select D10:D8 = 100b
    - Right Line In Select D2:D0 = 100b
- Unfortunately, the STAC9758 cannot mix Line In and Video at the same time.

Using Pins 16 and 17 as Line In for Video is the easiest method to use Video In on the STAC9758. The alternative, is to use Pins 16/17 as MIC, using the registers listed above, simple select the bit values to the desired input source.

9.0.13. Aux Volume (16h)

Default: 8808h.

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED		GL4	GL3	GL2	GL1	GR0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RMute	RESERVED		GR4	GR3	GR2	GR1	GR0

Bit(s)	Reset Value	R/W	Name	Description
15	1	RW	Mute	0 = no mute 1 = mute The channels to be affected are determined by the SPLITMUTE bit (Reg 72, Page 0, D6) If SPLITMUTE = 0 - both Left and Right channels are muted If SPLITMUTE = 1 - only the Left Channel is muted
14:13	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
12:8	08	RW	GL<4:0>	Left Aux Volume Control 00h = 00000b = +12.0 dB gain 01h = 00001b = +10.5 dB gain ..... 08h = 01000b = 0 dB - unity gain (default) ..... 1Fh = 11111b = -34.5 dB attenuation
7	0	RW	RMute	Mutes Right Channel independent of Left Channel 0=unmute 1=muted The SPLITMUTE bit (Reg 72 (Page 0), D6) must be set to 1 in order for the RMute bit to have an effect on the sound. The RMute bit is R/W. The RMute bit may be written and read regardless of the state of the SPLITMUTE bit.
6:5	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
4:0	08	RW	GR<4:0>	Right Aux Volume Control 00h = 00000b = +12.0 dB gain 01h = 00001b = +10.5 dB gain ..... 08h = 01000b = 0 dB - unity gain (default) ..... 1Fh = 11111b = -34.5 dB attenuation

9.0.14. PCMOut Volume (18h)

Default: 8808h.

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED		GL4	GL3	GL2	GL1	GR0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RMute	RESERVED		GR4	GR3	GR2	GR1	GR0

Bit(s)	Reset Value	R/W	Name	Description
15	1	RW	Mute	0 = no mute 1 = mute The channels to be affected are determined by the SPLITMUTE bit (Reg 72, Page 0, D6) If SPLITMUTE = 0 - both Left and Right channels are muted If SPLITMUTE = 1 - only the Left Channel is muted
14:13	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
12:8	08	RW	GL<4:0>	Left PCM Volume Control 00h = 00000b = +12.0 dB gain 01h = 00001b = +10.5 dB gain ..... 08h = 01000b = 0 dB - unity gain (default) ..... 1Fh = 11111b = -34.5 dB attenuation
7	0	RW	RMute	Mutes Right Channel independent of Left Channel 0=unmute 1=muted The SPLITMUTE bit (Reg 72 (Page 0), D6) must be set to 1 in order for the RMute bit to have an effect on the sound. The RMute bit is R/W. The RMute bit may be written and read regardless of the state of the SPLITMUTE bit.
6:5	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
4:0	08	RW	GR<4:0>	Right PCM Volume Control 00h = 00000b = +12.0 dB gain 01h = 00001b = +10.5 dB gain ..... 08h = 01000b = 0 dB - unity gain (default) ..... 1Fh = 11111b = -34.5 dB attenuation

NOTE: WDM Drivers normally leave Reg 18h set to 0808h (unity gain). It does not change during the Windows session. Instead, the Windows software mixer adjusts the Wave volume digitally.

9.0.15. Record Select (1Ah)

Default: 0000h (corresponding to Mic in)

Used to select the record source independently for right and left.

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED					SL2	SL1	SL0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED					SR2	SR1	SR0

Bit(s)	Reset Value	R/W	Name	Description
15:11	0	RO	RESERVED	BITS NOT USED, SHOULD READ BACK 0
10:8	0	RW	SL2:S	LEFT CHANNEL INPUT SELECT 00h = 000b = Mic mux This selects the output of the MicMux (Reg 66h) if Reg 20h, bit D8 = 0 then Mic L if Reg 20h, bit D8 = 1 then Mic R 001 = CD In (left) 010 = Not implemented (Mute input to mux) 011 = Aux In (left) 100 = Line In mux (left) This selects the output of the LineInMux (Reg 66h) 101 = Stereo Mix (left) 110 = Mono Mix 111 = Phone
7:3	0	RO	RESERVED	BITS NOT USED, SHOULD READ BACK 0
2:0	0	RW	SR2:SR0	RIGHT CHANNEL INPUT SELECT 00h = 000b = Mic mux This selects the output of the MicMux (Reg 66h) if Reg 20h, bit D8 = 0 then Mic R if Reg 20h, bit D8 = 1 then Mic L 001 = CD In (right) 010 = Not Implemented (Mute input to mux) 011 = Aux In (right) 100 = Line In mux (right) This selects the output of the LineInMux (Reg 66h) 101 = Stereo Mix (right) 110 = Mono Mix 111 = Phone

9.0.16. Record Gain (1Ch)

Default: 8000h (corresponding to 0 dB gain with mute on)

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED			GL3	GL2	GL1	GL0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RMute	RESERVED			GR3	GR2	GR1	GR0

Bit(s)	Reset Value	R/W	Name	Description
15	1	RW	Mute	0 = no mute 1 = mute The channels to be affected are determined by the SPLITMUTE bit (Reg 72, Page 0, D6) If SPLITMUTE = 0 - both Left and Right channels are muted If SPLITMUTE = 1 - only the Left Channel is muted
14:12	0	RO	RESERVED	BITS NOT USED, SHOULD READ BACK 0
11:8	0	RW	GL<3:0>	LEFT ADC VOLUME CONTROL 00h = 0000 = 0 dB gain 01h = 0001 = +1.5 dB gain .... 0Fh = 1111 = +22.5 dB gain
7	0	RW	RMute	Mutes Right Channel independent of Left Channel 0=unmute 1=muted The SPLITMUTE bit (Reg 72 (Page 0), D6) must be set to 1 in order for the RMute bit to have an effect on the sound. The RMute bit is R/W. The RMute bit may be written and read regardless of the state of the SPLITMUTE bit.
6:4	0	RO	RESERVED	BITS NOT USED, SHOULD READ BACK 0
3:0	0	RW	GR<3:0>	RIGHT ADC VOLUME CONTROL 00h = 0000 = 0 dB gain 01h = 0001 = +1.5 dB gain .... 0Fh = 1111 = +22.5 dB gain

NOTE: Most signals coming from external line-level sources will not need any additional gain. Signals coming from the MicMux (see Reg 66h) will have the Mic Boost values (0, 10, 20, or 30 dB) added to the values indicated by the GL and GR bits in Reg 1Ch

9.0.17. General Purpose (20h)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
POP	RESERVED	3D	RESERVED	DRSS1	DRSS0	MIX	MS
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
LOOPBACK	RESERVED						

Bit(s)	Reset Value	R/W	Name	Description
15	0	RW	POP	Pop bypass disables DAC-A digital 3-D only. This ensures that a recording of the DAC (through Stereo Mix) does not perform the 3D processing twice.
14	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
13	0	RW	3D	0 = 3D EFFECT DISABLED 1 = 3D EFFECT ENABLED
12	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
11:10	00	RW	DRSS <1:0>	DAC-A Double Rate Slot Select Rate Slot Select 00: PCM L, R n+1 data is on Slots 10-11 (default) 01: PCM L, R n+1 data is on slots 7, 8 10: Reserved 11: Reserved
9	0	RW	MIX	Mono Output select (0 = Mix, 1 = Mic)
8	0	RW	MS	Mic Select / Mic Swap
7	0	RW	LOOPBACK	1= ENABLES ADC to DAC LOOP BACK TEST 0= Loopback Disabled Each ADC output will go to all 3 DAC pairs.
6:0	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0

9.0.18. 3D Control (22h)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED				DP3	DP2	RESERVED	

Bit(s)	Reset Value	R/W	Name	Description
15:4	0	RO	RESERVED	BITS NOT USED, SHOULD READ BACK 0
3:2	0	RW	DP3,DP2	**LINE_OUT SEPARATION RATIO** DP3 DP2 effect 0 0 0 (OFF) 0 1 3 (LOW) 1 0 4.5 (MED) 1 1 6 (HIGH)
1:0	0	RO	RESERVED	BITS NOT USED, SHOULD READ BACK 0

This register is used to control the 3D stereo enhancement function, ***SigmaTel Surround 3D (SS3D),*** built into the AC'97 component. Note that register bits DP3-DP2 are used to control the separation ratios in the 3D control for LINE_OUT. ***SS3D*** provides for a wider soundstage extending beyond the normal 2-speaker arrangement. Note that the 3D bit in the general purpose register (20h) must be set to 1 to enable SS3D functionality to allow the bits in 22h to take effect.

The three separation ratios are implemented. The separation ratio defines a series of equations that determine the amount of depth difference (High, Medium, and Low) perceived during two-channel playback. The ratios provide for options to narrow or widen the soundstage.

9.0.19. Audio Interrupt and Paging (24h)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
I4	I3	I2	I1	I0	RESERVED		
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED				PG3	PG2	PG1	PG0

Bit(s)	Reset Value	R/W	Name	Description
15	0	RW	I4	0=Interrupt is clear 1=interrupt is set Interrupt event is cleared by writing a “1” to this bit. The interrupt bit will change regardless of condition of interrupt enable (I0) status. An interrupt in the GPI in slot 12 in the ACLink will follow this bit change when interrupt enable (I0) is unmasked.
14-13	0	RO	I3-I2	Interrupt Cause 00 = Reserved 01 = Sense Cycle Complete, sense info available. 10 = Change in GPIO input status 11 = Sense Cycle Complete and Change in GPIO input status. These bits will reflect the general cause of the first interrupt event generated. It should be read after interrupt status has been confirmed as interrupting. The information should be used to scan possible interrupting events in proper pages.
12	0	RW	I1	Sense Cycle 0 = Sense Cycle not in Progress 1 = Sense Cycle Start. Writing a “1” to this bit causes a sense cycle start if supported. If sense cycle is not supported this bit is read only.
11	0	RW	I0	Interrupt Enable 0 = Interrupt generation is masked. 1 = Interrupt generation is un-masked. The driver should not un-mask the interrupt unless ensured by the AC ‘97 controller that no conflict is possible with modem slot 12 - GPI functionality. Some AC’97 2.2 compliant controllers will not likely support audio codec interrupt infrastructure. In either case, S/W should poll the interrupt status after initiating a sense cycle and wait for Sense Cycle Max Delay to determine if an interrupting event has occurred.
10:4	0	RO	RESERVED	BITS NOT USED, SHOULD READ BACK 0
3:0	0	RW	PG3:PG0	Page Selector 00h = Vendor Specific 01h = Page ID 01 (See Section 9.3: page 79 for additional information on the Paging Registers) 02h-0Fh = Reserved Pages This register is used to select a descriptor of 16 word pages between registers 60h to 6Fh. Value 0h is used to select vendor specific space to maintain compatibility with AC’97 2.2 vendor specific registers. System S/W determines implemented pages by writing the page number and reading the value back. All implemented pages must be consecutive. (i.e., page 2h cannot be implemented without page 1h).

9.0.20. Powerdown Ctrl/Stat (26h)

Default: 000Fh

D15	D14	D13	D12	D11	D10	D9	D8
EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED				REF	ANL	DAC	ADC

Bit(s)	Reset Value	R/W	Name	Description
15	0	RW	EAPD	1 = Forces EAPD pad to VDDD 0 = Forces EAPD pad to GNDD
14	0	RW	PR6	0=Headphone Amp powered up 1=Headphone Amp powered down
13	0	RW	PR5	0=Digital Clk active 1=Digital Clk disable.
12	0	RW	PR4	0=digital active 1=Powerdown: PLL, AC-Link, Xtal oscillator; Forced low: bit clock, SDATA_IN Disabled: DSP clk, SPDIF clk
11	0	RW	PR3	0=VAG/VREF and VREFOUTare active 1=VAG/VREF and VREFOUT are powered down, and PR2 is asserted in analog block
10	0	RW	PR2	0=analog active 1=all signal path analog is powered down (VREFout and VAG still on, user should set PR0, PR1, PR6 prior to setting PR2)
9	0	RW	PR1	0=ALL DACs powered up 1=ALL DACs powered down PR1 is the global DAC powerdown, and powers down all DACs. PR1 is ORed with respective PR1, PRJ, PRK and PR_DAC_A bits
8	0	RW	PR0	0=ADC powered up 1=ADC powered down
7:4	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
3	1	RO	REF	VREF status 1 = VREF'S enabled
2	1	RO	ANL	ANALOG MIXERS, etc. Status 1 = analog mixers ready.
1	1	RO	DAC	DAC Status 1 = DAC ready to playback (Front DAC only) The PR_DAC_A bit is used to independently power down DAC-A
0	1	RO	ADC	ADC Status 1 = ADC ready to record

9.0.20.1. Ready Status

The lower half of this register is read only status, a "1" indicating that each subsection is "ready". Ready is defined as the subsection's ability to perform in its nominal state. When this register is written, the bit values that come in on AC-Link will have no effect on read only bits 0-7.

When the AC-Link "Codec Ready" indicator bit (SDATA_IN slot 0, bit 15) is a 1, it indicates that the AC-Link and AC'97 control and status registers are in a fully operational state. The AC'97 controller must further probe this Powerdown Control/Status Register to determine exactly which subsections, if any are ready. When this register is written, the bit values that come in on AC-Link will have no effect on read only bits 0-7.

9.0.20.2. Powerdown Controls

The STAC9758/59 is capable of operating at reduced power when no activity is required. The state of power down is controlled by the Powerdown Register (26h). See the section "Low Power Modes" for more information.

9.0.20.3. External Amplifier Power Down Control Output

The EAPD bit 15 of the Powerdown Control/Status Register (Index 26h) directly controls the output of the EAPD output, pin 47, and produces a logical "1" when this bit is set to logic high. This function is used to control an external audio amplifier power down. EAPD = 0 places approximately 0V on the output pin, enabling an external audio amplifier. EAPD = 1 places approximately DVdd on the output pin, disabling the external audio amplifier. Audio amplifiers that operate with reverse polarity will likely require an external inverter to maintain software driver compatibility.

EAPD can also act as a GPIO or SPDIF_IN. See Section 9.1.1: page 75. The GPIO controls in Section 9.1: page 75 have no effect on EAPD.

9.0.21. Extended Audio ID (28h)

Default: 0BC7h

D15	D14	D13	D12	D11	D10	D9	D8
ID1	ID0	RESERVED		REV1	REV0	AMAP	LDAC
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
SDAC	CDAC	DSA1	DSA0	RESERVED	SPDIF	DRA	VRA

The Extended Audio ID register is a read only register except for bits D4 and D5. ID1 and ID0 echo the configuration of the codec as defined by the programming of pin 46 externally. ID0 is always a “0” for the 9758. “00” returned defines the codec as the primary codec, while “10” code identifies the codec as the secondary codec. The AMAP bit, D9, will return a 1 indicating that the codec supports the optional “AC’97 2.3 compliant AC-link slot to audio DAC mappings. The default condition assumes that 0, 0 are loaded in the DSA0 and DSA1 bits of the Extended Audio ID (Index 28h). With 0s in the DSA1 and DSA0 bits, the codec slot assignments are as per the AC’97 specification recommendations. If the DSA1 and DSA0 bits do not contain 0s, the slot assignments are as per the table in the section describing the Extended Audio ID (Index 28h). The VRA bit, D0, will return a 1 indicating that the

codec supports the optional variable sample rate conversion as defined by the AC'97 specification.

Bit	Reset Value	R/W	Name	Function
15:14	00 or 10	RO	ID [1,0]	0,0=XTAL_OUT grounded (note 1) CID1#,CID0#=XTAL_OUT crystal or floating
13:12	00	RO	RESERVED	BITS NOT USED, SHOULD READ BACK 00
11:10	10	RO	REV[1:0]	Indicates Codec is AC'97 Rev 2.3 compliant
9	1	RO	AMAP	Multi-channel slot support (Always = 1)
8	1	RO	LDAC	Low Frequency Effect DAC Supported
7	1	RO	SDAC	Surround DACs Supported
6	1	RO	CDAC	Center channel DAC Supported
5:4	00	RW	DSA [1,0]	DAC slot assignment See DSA table below. The DSA bits for DAC-A are ignored when Double Rate Audio DRA is used. Slots 3&4 are used instead. The DRSS bits indicate which secondary slots to use. DAC-B and DAC-C are unaffected by the DRA bit.
3	0	RO	RESERVED	RESERVED
2	1	RO	SPDIF	0=SPDIF pulled high on reset, SPDIF disabled 1=default, SPDIF enabled (Note 2)
1	1	RO	DRA	Double Rate Audio Supported
0	1	RO	VRA	Variable sample rates supported (Always = 1)

1. External CID pin status (from analog) these bits are the logical inversion of the pin polarity (pin 46). These bits are zero if XTAL_OUT is grounded with an alternate external clock source in primary mode only. Secondary mode can either be through BIT CLK driven or 24MHz clock driver, with XTAL_OUT floating.
2. **If pin 48 is held high at powerup, this bit will be held to zero, to indicate the SPDIF is not available. Tie to ground with a 10K resistor to ensure SPDIF is enabled.**

AMAP Defaults					
Codec ID	**Function**	**DAC1**	**DAC2**	**DAC3**	**SPDIF**
ALL	6-ch Primary w/ SPDIF	3 & 4	7 & 8	6 & 9	10 & 11

DSA Assignment Table			
DSA1, DSA0	DACs 1,2	DACs 3,4	DACs 5,6
00 (default)	3&4	7&8	6&9
01	7&8	6&9	10&11
10	6&9	10&11	3&4
11	10&11	3&4	7&8

9.0.22. Extended Audio Control/Status (2Ah)

Default: 05F0h

D15	D14	D13	D12	D11	D10	D9	D8
VCFG	RESERVED	PRK	PRJ	PRI	SPCV	RESERVED	LDAC
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
SDAC	CDAC	SPSA1	SPSA0	RSRVD	SPDIF	DRA	VRA enable

1. If pin 48 is held high at powerup, the SPDIF is not available and bits D15:D1 can not be written and will read back zero..

Bit(s)	Reset Value	R/W	Name	Description
15	0	RW	VCFG	Determines the SPDIF transmitter behavior when data is not being transmitted. When asserted, this bit forces the deassertion of the SPDIF “Validity” flag, which is bit 28 transmitted by the SPDIF sub-frame. The “V” bit is defined in the SPDIF Control Register (Reg 3Ah). If "V"=1 and "VCFG" = 0, then for each SPDIF sub-frame (Left & Right), bit<28> "Validity" flag reflects whether or not an internal CODEC transmission error has occurred. Specifically an internal CODEC error should result in the "Validity" flag being set to "1". If "V"=0 and "VCFG" = 1, In the case where the SPDIF transmitter does not receive a valid sample from the AC'97 controller, (Left or Right), the SPDIF transmitter should set the "Validity" flag to "0" and pad the "Audio Sample Word" with "0"s for sub-frame in question. If a valid sample (Left or Right) was received and successfully transmitted, the "Validity" flag should be "0" for that sub-frame. Default state, coming out of reset, for "V" and "VCFG" should be 0 and 0. These bits should be settable via driver .inf options.
14	0	RO	RESERVED	RESERVED
13	0	RW	PRK	0=PCM LFE DACs on 1=PCM LFE DACs off
12	0	RW	PRJ	0=PCM Surround DACs on 1=PCM Surround DACs off
11	0	RW	PRI	0=PCM Center DAC on 1=PCM Center DAC off
10	1	RO	SPCV	0 = invalid SPDIF configuration 1 = valid SPDIF configuration
9	0	RO	RESERVED	RESERVED
8	1	RO	LDAC	0=PCM LFE DAC is not ready 1=PCM LFE DAC is ready
7	1	RO	SDAC	0=PCM Surround DAC is not ready 1=PCM Surround DAC is ready
6	1	RO	CDAC	0=PCM Center DAC is not ready 1=PCM Center DAC is ready

Bit(s)	Reset Value	R/W	Name	Description
5:4	11	RW	SPSA1:SPSA0	SPDIF slot assignment 00 = left slot 3, right slot 4 01 = left slot 7, right slot 8 10 = left slot 6, right slot 9 11 = left slot 10, right slot 11 The DRS (Double Rate SPDIF) bit causes the primary data to be taken from slots 3&4. The secondary data is taken from the slots indicated by SPSA. If SPSA bits are set to 00 (slot pair 3/4) and DRS bit (Double Rate SPDIF) is set to 1, then the 20-bit data to DAC-A will be doubled. This will not sound particularly bad, but is an operating mode which provides little benefit.
3	0	RO	RESERVED	RESERVED
2	0	RW	SPDIF	0 = disables SPDIF (SPDIF_OUT is high Z) (note 1) 1 = enable SPDIF SPDIF is a control bits for Reg 3Ah. This bit must be set low, i.e. SPDIF disabled, in order to write to Reg 3Ah Bits D15,D13:D0.
1	0	RW	DRA	Double Rate Audio 0=disabled 1=enabled When DRA bit is set, then the DSA bits (Reg 28, Bits D5:D4) have no effect. Data from PCM L and PCM R in output slots 3 and 4 is used in conjunction with PCM L (n+1) and PCM R (n+1) data , to provide DAC streams at twice the sample rate designated by the PCM Front Sample Rate Control Register. The slots on which the (n+1) data is transmitted on is indicated by the DRSS[1:0] bits in the General Purpose Register 20h. Note that DRA can be used without VRA, in that case the converter rates are forced to 96kHz if DRA=0.
0	0	RW	VRA Enable	Variable Rate Audio Enable 0 = Disabled DAC and ADC set to 48kHz Reg 2Ch, Reg 2Eh, Reg 30h & Reg 32h all read back BB80h 1 = Enabled Reg 2Ch, Reg 2Eh, Reg 30h & Reg 32h control the various DAC and ADCsample rates

9.0.22.1. Variable Rate Audio Enable

The Extended Audio Status Control register also contains one active bit to enable or disable the Variable Sampling Rate capabilities of the DACs and ADCs. If VRA Enable (Reg 20h, bit D0) is 1, the variable sample rate control registers (2Ch, 2Eh, 30h, and 32h) are active, and “on-demand” slot data required transfers are allowed. If the VRA bit is 0, the DACs and ADCs will operate at the default 48 kHz data rate.

The STAC9758/59 supports “on-demand” slot request flags. These flags are passed from the codec to the AC’97 controller in every audio input frame. Each time a slot request flag is set (active low) in a given audio frame, the controller will pass the next PCM sample for the corresponding slot in the audio frame that immediately follows. The VRA Enable bit must be set to 1 to enable “on-demand” data transfers. If the VRA Enable bit is not set, the codec will default to 48 kHz transfers and every audio frame will include an active slot request flag. Data is transferred every frame in this case.

For variable sample rate output, the codec examines its sample rate control registers, the state of the FIFOs, and the incoming SDATA_OUT tag bits at the beginning of each audio output frame to determine which SLOTREQ bits to set active (low). SLOTREQ bits are asserted during the current audio input frame for active output slots which will require data in the next audio output frame.

For variable sample rate input, the tag bit for each input slot indicates whether valid data is present or not. Thus, even in variable sample rate mode, the codec is always the master: for SDATA_IN (codec to controller), and the codec sets the TAG bit. For SDATA_OUT (controller to codec), the codec sets the SLOTREQ bit and then checks for the TAG bit in the next frame. Whenever VRA is set to 0 the PCM rate registers (2Ch, 2Eh, 30h, and 32h) are overwritten with BB80h (48 kHz).

9.0.22.2. SPDIF Output

The SPDIF bit in the Extended Audio Status Control Register is used to enable and disable the SPDIF output functionality within the STAC9758/59. If the SPDIF Output bit is set to a 1, then the SPDIF Output function is enabled.

9.0.22.3. SPCV (SPDIF Output Configuration Valid)

The SPCV bit is read only and indicates whether or not the SPDIF Output system is set up correctly. When SPCV is a 0, it indicates the system configuration is invalid and valid if it is a 1.

9.0.22.4. SPSA1, SPSA0 (SPDIF Output Slot Assignment)

SPSA1 and SPSA0 combine to provide the slot assignments for the SPDIF output data. STAC9758/59 is AMAP compliant as per the following table.

AMAP Defaults					
Codec ID	**Function**	**DAC1**	**DAC2**	**DAC3**	**SPDIF**
ALL	6-ch Primary w/ SPDIF	3 & 4	7 & 8	6 & 9	10 & 11

Table 19. AMAP compliant

9.0.23. PCM DAC Rate Registers

The internal sample rate for the DACs and ADCs are controlled by the value in these read/write registers. Each register that contains a 16-bit unsigned value between 0 and 65535 which represents the conversion rate in Hz.

In VRA mode (Reg 2Ah Bit D0 = 1), if the value written to these registers is supported, that value will be echoed back when read, otherwise the closest (higher in the case of a tie) sample rate is supported and returned. Per PC 99 / PC 2001 specification, independent sample rates are supported for record and playback.

Whenever VRA is set to 0, all PCM DAC and ADC rate registers will be loaded with BB80h (48 kHz).

If VRA is set to a 0, any write to this address will be ignored and the rate remains at 48KHz.

Sample Rate	SR15-SR0 Value
8.000 kHz	1F40h
11.025 kHz	2B11h
16.000 kHz	3E80h
22.050 kHz	5622h
32.000 kHz	7D00h
44.100 kHz	AC44h
48.000 kHz	BB80h

Table 20. Hardware Supported Sample Rates

9.0.24. PCM DAC Rate (2Ch)

Controls DAC-A (Front) and DAC-CL (Center)

Default: BB80h (see table 20: page 71)

D15	D14	D13	D12	D11	D10	D9	D8
SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0

9.0.25. PCM Surround DAC Rate (2Eh)

Controls DAC-B (Surround)

Default: BB80h (see table 20: page 71)

D15	D14	D13	D12	D11	D10	D9	D8
SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0

9.0.26. PCM LFE DAC Rate (30h)

Controls DAC-CR (LFE)

Default: BB80h (see table 20: page 71)

D15	D14	D13	D12	D11	D10	D9	D8
SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0

9.0.27. PCM LR ADC Rate (32h)

Default: BB80h (see table 20: page 71)

D15	D14	D13	D12	D11	D10	D9	D8
SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0

9.0.28. Center/LFE Volume (36h)

Default: 8080h

D15	D14	D13	D12	D11	D10	D9	D8
MUTE	RESERVED	LFE5	LFE4	LFE3	LFE2	LFE1	LFE0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
MUTE	RESERVED	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0

Bit(s)	Reset Value	R/W	Name	Description
15	1	RW	MUTE	0 = LFE not muted 1 = LFE muted
14	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
13	0	WO	LFE5	If a 1 is written to this bit, then LFE<4:0> is loaded with 11111b. This bit always reads 0.
12:8	0	RW	LFE[4:0]	00h = 00000b = 0.0 dB attenuation 01h = 00001b = -1.5 dB attenuation ..... 1Fh = 11111b = -46.5 dB attenuation
7	1	RW	MUTE	0 = CENTER not muted 1 = CENTER muted
6	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
5	0	WO	CNT5	If a 1 is written to this bit, then CNT<4:0> is loaded with 11111b. This bit always reads 0.
4:0	0	RW	CNT[4:0]	00h = 00000b = 0.0 dB attenuation 01h = 00001b = -1.5 dB attenuation ..... 1Fh = 11111b = -46.5 dB attenuation

9.0.29. Surround Volume (38h)

Default: 8080h

D15	D14	D13	D12	D11	D10	D9	D8
MUTE	RESERVED	LSR5	LSR4	LSR3	LSR2	LSR1	LSR0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
MUTE	RESERVED	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0

Bit(s)	Reset Value	R/W	Name	Description
15	1	RW	MUTE	0 = Left Surround not muted 1 = Left Surround muted
14	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
13	0	WO	LSR5	If a 1 is written to this bit, then LSR<4:0> is loaded with 11111b. This bit always reads 0.
12:8	0	RW	LSR[4:0]	00h = 00000b = 0.0 dB attenuation 01h = 00001b = -1.5 dB attenuation ..... 1Fh = 11111b = -46.5 dB attenuation
7	1	RW	MUTE	0 = Right Surround not muted 1 = Right Surround muted
6	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
5	0	WO	RSR5	If a 1 is written to this bit, then RSR<4:0> is loaded with 11111b. This bit always reads 0.
4:0	0	RW	RSR[4:0]	00h = 00000b = 0.0 dB attenuation 01h = 00001b = -1.5 dB attenuation ..... 1Fh = 11111b = -46.5 dB attenuation

9.0.30. SPDIF Control (3Ah)

Default: 2000h

D15	D14	D13	D12	D11	D10	D9	D8
V	DRS	SPSR1	SPSR2	L	CC6	CC5	CC4
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
CC3	CC2	CC1	CC0	PRE	COPY	/AUDIO	PRO

Bit(s)	Reset Value	R/W	Name	Description
15	0	RW	V	Validity: This bit affects the "Validity" flag, bit<28> transmitted in each SPDIF subframe, and enables the SPDIF transmitter to maintain connection during error or mute conditions. Subframe bit<28> = "0" indicates that data is valid for conversion at the receiver, "1" indicates invalid data (not suitable for conversion at the receiver). If "V" = 1, then each SPDIF subframe (Left & Right) should have bit<28> "Validity" flag = 1 or set based on the assertion or de-assertion of the AC '97 "VFORCE" bit within the Extended Audio Status and Control Register (D15, register 2Ah).
14	0	RW	DRS	Double Rate SPDIF 0 = not enabled 1 = enables SPDIF Sample Rates of 64 kHz, 88.2 kHz, and 96 kHz When DRS is enabled, the SPDIF transmitter uses AC-link slots 3&4 plus the slot pair specified in the SPSA bits (Reg 2A, Bits D5:D4) to supply data at Fs = 64, 88.2 or 96 kHz. A total of four slots are used for a stereo pair when operating in this mode. The first stereo pair to be played is contained in slots 3&4, and the second pair is contained in the slots specified by the SPSA bits. The SPCV bit must indicate a valid configuration. The STAC9758/59 automatically determines the correct channel status bits for Fs from DRS and SPSR and inserts them as necessary. The Controller or Driver should perform write followed by read to determine if DRS is supported.
13:12	10	RW	SPSR[1,0]	SPDIF and ADAT Sample Rate. 00 44.1 kHz Rate 01 Reserved 10 48 kHz Rate (default) 11 32 kHz Rate When DRS (D14 is set), SPDIF (but not ADAT) will operate at 00 88.2 kHz 01 Reserved 10 96 kHz (default) 11 64 kHz
11	0	RW	L	Generation Level is defined by the IEC standard, or as appropriate.
10:4	0	RW	CC[6, 0]	Category Code is defined by the IEC standard or as appropriate by media.
3	0	RW	PRE	0 = 0 usec Pre-emphasis 1 = Pre-emphasis is 50/15 usec
2	0	RW	COPY	0 = Copyright not asserted 1 = Copyright is asserted
1	0	RW	/AUDIO	0 = PCM data 1 = Non-Audio or non-PCM format
0	0	RW	PRO	0 = Consumer use of the channel 1 = Professional use of the channel

9.1. General Purpose Input & Outputs

9.1.1. EAPD

EAPD can act as a GPIO, but is unaffected by the following registers. To use EAPD as a GPIO, use Register 74h, the EAPD Access Register located in Section 9.3.19: page 96. Additional information about EAPD can also be found in Section 9.0.20.3: page 66.

9.1.2. GPIO Pin Definitions

GPIO pins are programmable to have input/output functionality. The data values (status) for these pins are all in one register with input/output configuration in a separate register. Control of GPIO pins configured for output is achieved by setting the corresponding bit in output slot 12; status of GPIO pins configured for input is returned on input slot 12. The Codec must constantly set the GPIO pins that are configured for output, based upon the value of the corresponding bit position of the control slot 12. The Codec should ignore output slot 12 bits that correspond to GPIO control pins configured as inputs. The Codec must constantly update status on input slot 12, based upon the logic level detected at each GPIO pin configured for input. A GPIO output pin value that is written via slot 12 in the current frame won't affect the GPIO status that is returned in that particular write frame.

This slot 12-based control/status protocol minimizes the latency and complexity, especially for host-based Controllers and host data pump software, and provides high speed monitoring and control, above what could be achieved with command/status slots. For host-based implementations most AC '97 registers can be shadowed by the driver in order to provide immediate response when read by the processor, and GPIO pins configured as inputs should be capable of triggering an interrupt upon a change of status.

The AC-link request for GPIO pin status is always delayed by at least one frame time. Read-Modify-Writes across the AC-link will thus incur latency issues and must be accounted for by the software driver or AC '97 Digital Controller firmware. PCI retries should be kept to a minimum wherever possible.

9.1.3. GPIO Pin Implementation

The GPIOs are tri-stated to a high impedance state on power-on or a cold reset. It is up to the AC '97 Digital Controller to first enable the output after setting it to the desired state. GPIO 0 and GPIO 1 are now on pins 33 and 34 (respectively) and powered from the analog supply. When using these pins in an application, care must be taken to reduce the risk of injecting noise into the analog section. Also, GPIO0 and GPIO1 will not be available when the analog supply is removed.

9.1.4. Extended Modem Status and Control Register (3Eh)

Default: 0100h

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED							PRA
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED							GPIO

Bit(s)	Reset Value	R/W	Name	Description
15:9	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
8	1	RW	PRA	0=GPIO powered up / enabled 1=GPIO powered down / disabled
7:1	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
0	0	RO	GPIO	0 = GPIO not ready (powered down) 1 = GPIO ready (powered up) (This is just bit D8 inverted)

9.1.5. GPIO Pin Configuration Register (4Ch)

Default: 000Fh

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED				GC3 (GPIO3)	GC2 (GPIO2)	GC1 (GPIO1)	GC0 (GPIO0)

Bit(s)	Reset Value	R/W	Name	Description
15:4	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
3	1	RW	GC3	0 = GPIO3 configured as output 1 = GPIO3 configured as input
2	1	RW	GC2	0 = GPIO2 configured as output 1 = GPIO2 configured as input
1	1	RW	GC1	0 = GPIO1 configured as output 1 = GPIO1 configured as input
0	1	RW	GC0	0 = GPIO0 configured as output 1 = GPIO0 configured as input

9.1.6. GPIO Pin Polarity/Type Register (4Eh)

Default: FFFFh

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED				GP3 (GPIO3)	GP2 (GPIO2)	GP1 (GPIO1)	GP0 (GPIO0)

Bit(s)	Reset Value	R/W	Name	Description
15:4	FFFh	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
3	1	RW	GP3	0 = GPIO3 Input Polarity Inverted, CMOS output drive. 1 = GPIO3 Input Polarity Non-inverted, Open-Drain output drive.
2	1	RW	GP2	0 = GPIO2 Input Polarity Inverted, CMOS output drive. 1 = GPIO2 Input Polarity Non-inverted, Open-Drain output drive.
1	1	RW	GP1	0 = GPIO1 Input Polarity Inverted, CMOS output drive. 1 = GPIO1 Input Polarity Non-inverted, Open-Drain output drive.
0	1	RW	GP0	0 = GPIO0 Input Polarity Inverted, CMOS output drive. 1 = GPIO0 Input Polarity Non-inverted, Open-Drain output drive.

9.1.7. GPIO Pin Sticky Register (50h)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED				GS3 (GPIO3)	GS2 (GPIO2)	GS1 (GPIO1)	GS0 (GPIO0)

Bit(s)	Reset Value	R/W	Name	Description
15:4	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
3	0	RW	GS3	0 = GPIO3 Non Sticky configuration. 1 = GPIO3 Sticky configuration.
2	0	RW	GS2	0 = GPIO2 Non Sticky configuration. 1 = GPIO2 Sticky configuration.
1	0	RW	GS1	0 = GPIO1 Non Sticky configuration. 1 = GPIO1 Sticky configuration.
0	0	RW	GS0	0 = GPIO0 Non Sticky configuration. 1 = GPIO0 Sticky configuration.

9.1.8. GPIO Pin Mask Register (52h)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED				GW3 (GPIO3)	GW2 (GPIO2)	GW1 (GPIO1)	GW0 (GPIO0)

Bit(s)	Reset Value	R/W	Name	Description
15:4	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
3	0	RW	GW3	0 = GPIO3 interrupt not passed to GPIO_INT slot 12. 1 = GPIO3 interrupt is passed to GPIO_INT slot 12.
2	0	RW	GW2	0 = GPIO2 interrupt not passed to GPIO_INT slot 12. 1 = GPIO2 interrupt is passed to GPIO_INT slot 12.
1	0	RW	GW1	0 = GPIO1 interrupt not passed to GPIO_INT slot 12. 1 = GPIO1 interrupt is passed to GPIO_INT slot 12.
0	0	RW	GW0	0 = GPIO0 interrupt not passed to GPIO_INT slot 12. 1 = GPIO0 interrupt is passed to GPIO_INT slot 12.

9.1.9. GPIO Pin Status Register (54h)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED				GI3 (GPIO3)	GI2 (GPIO2)	GI1 (GPIO1)	GI0 (GPIO0)

Bit(s)	Reset Value	R/W	Name	Description
15:4	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
3	x	RW	GI3	reads back value on GPIO3. writing 0 will clear GPIO3 sticky bit if set and enabled. writing 1 does nothing.
2	x	RW	GI2	reads back value on GPIO2. writing 0 will clear GPIO2 sticky bit if set and enabled. writing 1 does nothing.
1	x	RW	GI1	reads back value on GPIO1. writing 0 will clear GPIO1 sticky bit if set and enabled. writing 1 does nothing.
0	x	RW	GI0	reads back value on GPIO0. writing 0 will clear GPIO0 sticky bit if set and enabled. writing 1 does nothing.

9.2. Extended Codec Registers Page Structure Definition

Registers 60h-68h are the Extended Codec Registers: These registers allow for the definition of further capabilities. These bits provide a paged address space for extended codec information. The Page Selector bits in the Audio Interrupt and Paging register (Register 24h bits 3:0) control the page of information viewed through this page window.

9.2.1. Extended Registers Page 00

Page 00 of the Extended Codec Registers is reserved for vendor specific use. Driver writers should not access these registers unless the Vendor ID register has been checked first to ensure that the vendor of the AC '97 component has been identified and the usage of the vendor defined registers understood.

9.2.2. Extended Registers Page 01

The usage of Page 01 of the Extended Codec Registers is defined in Register 24h found in Section 9.0.19: page 64.

9.2.3. Extended Registers Page 02, 03

Pages 02 and 03 of the Extended Codec Registers are reserved for future use.

9.3. STAC9758/59 Paging Registers

The AC'97 Specification Rev 2.3 uses a paging mechanism in order to increase the number of registers. The registers currently used in the paging are 60h to 6Eh. Additional information about the Extended Codec Registers, please refer to Section 9.2: page 79.

One of two pages can be made active at any time, set in Register 24h. Register 24h is the Audio Interrupt and Paging Register. Additional details about Register 24h is located in Section 9.0.19: page 64.

If page 00h is active, registers 60h to 6Eh are Vendor Specific.

If page 01h is active, registers 60h to 6Eh have the following functionality:

Reg	NAME	FUNCTION	Location
60h	Codec Class/Revision	Provides the Codec Class and a Vendor specified revision identifier.	9.3.2: page 80
62h	PCI SVID	Allows for population by the system BIOS to identify the PCI Sub System Vendor ID.	9.3.4: page 82
64h	PCI SSID	Allows for population by the system BIOS to identify the PCI Sub System ID.	9.3.6: page 83
66h	Function Select	Provides the type of audio function being selected and which jack conductor the selected value is measured from.	9.3.8: page 85
68h	Function Information	Includes information about Gain, Inversion, Buffer delays, Information Validity, and Function Information presence.	9.3.10: page 87
6Ah	Sense Register	Includes information about the connector/jack location, Input verses Output sensing, the Order of the sense results, and the SigmaTel specifc sense results.	9.3.12: page 90
6Ch	DAC Slot Mapping	Allows the controlling software to modify the default slot to the DAC mappings.	9.3.14: page 91
6Eh	ADC Slot Mapping	Allows the controlling software to modify the default slot to the ADC mappings.	9.3.16: page 94

9.3.1. SPDIF_In Status 1 Register (60h, Page 00h)

Register 24h must be set to Page 00h to access this register.

Default:0000h

D15	D14	D13	D12	D11	D10	D9	D8
LVL	CC6	CC5	CC4	CC3	CC2	CC1	CC0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
MODE1	MODE0	PRE2	PRE1	PRE0	CPY	/AUD	PRO

First of 2 registers that echo the status bits taken from the SPDIF input stream header. All bits relate directly to the defined header bits for IEC60958. No translation or inversion necessary.

Bit(s)	Reset Value	R/W	Name	Description
15	0	RO	LVL	Generation level
14:8	0	RO	CC<6:0>	Category Code IEC spec " The category code indicates the kind of equipment that generates the digital audio interface signal."
7:6	0	RO	Mode<1:0>	Mode
5:3	0	RO	PRE<2:0>	Pre emphesis
2	0	RO	CPY	COPY
1	0	RO	/AUD	Non PCM / PCM 0= PCM data 1= non PCM (AC3). If SPDIF is routed to DAC-B, this will mute DAC-B.
0	0	RO	PRO	Professional / consumer 0= consumer 1= professional

9.3.2. Codec Class/Rev (60h Page 01h)

Register 24h must be set to Page 01h to access this register.

Default: 18xxh

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED			CL4	CL3	CL2	CL1	CL0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RV7	RV6	RV5	RV4	RV3	RV2	RV1	RV0

Bit(s)	Reset Value	R/W	Name	Description
15:13	0	RO	RESERVED	RESERVED-NOT DEFINED
12:8	*	RO	CL4:CL0	Codec Compatibility Class (RO) This is a codec vendor specific field to define s/w compatibility for the codec. S/W read this field together with codec vendor ID (reg 7C-7Eh) to determine vendor specific programming interface compatibility. S/w can rely on vendor specific register behavior to be compatible among vendor codecs of the same class. 00h - Field not implemented. 01h-1Fh - Vendor specific compatibility class code
7:0	**	RO	RV7:RV0	Revision ID: (RO) This register specifies a device specific revision identifier. The value is chosen by the vendor. Zero is an acceptable value. This field should be viewed as a vendor defined extension to the codec ID. This number changes with new codec stepping of the same codec ID.

9.3.3. SPDIF_In Status 2 Register (62h, Page 00h)

Register 24h must be set to Page 00h to access this register. Second of two registers that echo the status bits from the SDATA_IN header.

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
SP_VAL	RESERVED	CA1	CA0	FS3	FS2	FS1	FS0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
CN3	CN2	CN1	CN0	SN3	SN2	SN1	SN0

Bit(s)	Reset Value	R/W	Name	Description
15	0	RO	SP_VAL	0 = SPDIF Valid 1 = SPDIF Invalid Validity: This bit affects the "Validity" flag, bit<28> transmitted in each SPDIF subframe, and enables the SPDIF transmitter to maintain connection during error or mute conditions. Subframe bit<28> = "0" indicates that data is valid for conversion at the receiver, "1" indicates invalid data (not suitable for conversion at the receiver). If either SPDIF subframe bit 28 validity flag = 1, then this field is set to invalid, equal 1.
14	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
13:12	00	RO	CA<1:0>	Clock accuracy 00 = Level II 01 = Level I 10= Level III 11= Reserved
11:8	0000	RO	FS<3:0>	Sample Rate 0000= 44.1 kHz 0100= 48 kHz 1100= 32 kHz All other combinations are reserved and shall not be used until further defined (IEC spec).
7:4	0	RO	CN<3:0>	Channel Number (audio channel) 0000= do not take into account 1000= A (left channel for stereo channel format) 0100= B (right channel for stereo channel format) 1100= C ..... 1111= O
3:0	0	RO	SN<3:0>	Source Number 0000= do not take into account 1000= 1 0100= 2 1100= 3 ..... 1111= 15

9.3.4. PCI SVID (62h Page 01h)

Register 24h must be set to Page 01h to access this register.
Default: FFFFh

D15	D14	D13	D12	D11	D10	D9	D8
PVI15	PVI14	PVI13	PVI12	PVI11	PVI10	PVI9	PVI8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PVI7	PVI6	PVI5	PVI4	PVI3	PVI2	PVI1	PVI0

Bit(s)	Reset Value	R/W	Name	Description
15:0	FFFFh	RW	PVI15:PVI0	PCI Sub System Vendor ID: This field provides the PCI Sub System Vendor ID of the Audio or Modem Sub Assembly Vendor (i.e., CNR manufacturer, Motherboard Vendor). This is NOT the codec vendor PCI Vendor ID, nor the AC '97 controller PCI Vendor ID. If data is not available, returns FFFFh.

9.3.5. Universal Jack™ Output Select (64h, Page 00h)

Register 24h must be set to Page 00h to access this register.
Default: D794h

D15	D14	D13	D12	D11	D10	D9	D8
CSEN	CS1	CS0	RSEN	RS1	RS0	FSEN	FS1
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
FS0	LSEN	LS1	LS0	MSEN	MS1	MS0	RESERVED

Bit(s)	Reset	R/W	Name	Description
15	1	RW	CSEN	Pin 43/44 output enable (0 = pad powered down)
14:13	10	RW	CS[1:0]	Pins 43/44 (“Center/LFE” in default 6ch mode) 00= Front (DAC-A)...Volume 0x04 01= Rear (DAC-B)...Volume 0x38 10= CTR/LFE (DAC-C)...Volume 0x36 11= Mixer Out...Volume= 0x02
12	1	RW	RSEN	Pin 39/41 output enable
11:10	01	RW	RS[1:0]	Pins 39/41 (“Rear” in 6ch default mode) 00= Front (DAC-A)...Volume 0x04 01= Rear (DAC-B)...Volume 0x38 10= CTR/LFE (DAC-C)...Volume 0x36 11= Mixer Out...Volume= 0x02
9	1	RW	FSEN	Pin 35/36 output enable (0 = pad powered down)
8:7	11	RW	FS[1:0]	Line_Out = Pins 35/36 00= Front (DAC-A)...Volume 0x04 01= Rear (DAC-B)...Volume 0x38 10= CTR/LFE (DAC-C)...Volume 0x36 11= Mixer Out...Volume= 0x02
6	0	RW	LSEN	Pin 23/24 output enable
5:4	01	RW	LS[1:0]	Line-In = Pins 23/24 00= Front (DAC-A)...Volume 0x04 01= Rear (DAC-B)...Volume 0x38 10= CTR/LFE (DAC-C)...Volume 0x36 11= Mixer Out...Volume= 0x02
3	0	RW	MSEN	Pin21/22 output enable (0 = pad powered down)
2:1	10	RW	MS{1:0]	Mic = Pins 21/22 00= Front (DAC-A)...Volume 0x04 01= Rear (DAC-B)...Volume 0x38 10= CTR/LFE (DAC-C)...Volume 0x36 11= Mixer Out...Volume= 0x02
0	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0

Each output capable pin can have 4 sources: DAC-A, DAC-B, DAC-C, and Mixer Out. Each may be disabled/ tristated for use as an input. The 3 select bits work as follows:

xSEN	xS1	xS0	Resource	Volume Control Register
1	0	0	Front (DAC-A)	0x04
1	0	1	Rear (DAC-B)	0x38
1	1	0	CTR/LFE (DAC-C)	0x36
1	1	1	MIXER OUT	0x02
0	x	x	DISABLED	

9.3.6. PCI SSID (64h Page 01h)

Register 24h must be set to Page 01h to access this register.

Default: FFFFh

D15	D14	D13	D12	D11	D10	D9	D8
PI15	PI14	PI13	PI12	PI11	PI10	PI9	PI8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0

Bit(s)	Reset Value	R/W	Name	Description
15:0	FFFFh	RW	PI15:PVI0	PCI: This field provides the PCI Sub System ID of the Audio or Modem Sub Assembly (i.e., CNR Model, Motherboard SKU). This is NOT the codec vendor PCI ID, nor the AC '97 controller PCI ID. Information in this field must be available for AC '97 controller reads when codec ready is asserted in AC link.If data is not available, returns FFFFh.

9.3.7. *Universal Jack™ Input Select (66h, Page 00h)*

Register 24h must be set to Page 00h to access this register.

Default: 0201h

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED					LI2	LI1	LI0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED					MI2	MI1	MI0

Bit(s)	Reset Value	R/W	Name	Description
15:11	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
10:8	010	RW	LI[2:0]	Line Input Selector Determines which pair of input pins is routed to the input of the Line In section 00h = 000b = Pins 16 & 17 MIC2_L, MIC2_R 01h = 001b = Pins 21 & 22 MIC1_L, MIC1_R 02h = 010b = Pins 23 & 24 LINE_IN_L, LINE_IN_R 03h = 011b = Pins 35 & 36 FRONT_L, FRONT_R 04h = 100b = Pins 39 & 41 SURR_L, SURR_R 05h = 101b = Pins 43 & 44 CTR, LFE 06h = 110b = MUTE 07h = 111b = MUTE
7:3	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
2:0	001	RW	MI[2:0]	Microphone Input Selector Determines which pair of input pins is routed to the input of the Microphone Preamp 00h = 000b = Pins 16 & 17 MIC2_L, MIC2_R 01h = 001b = Pins 21 & 22 MIC1_L, MIC1_R 02h = 010b = Pins 23 & 24 LINE_IN_L, LINE_IN_R 03h = 011b = Pins 35 & 36 FRONT_L, FRONT_R 04h = 100b = Pins 39 & 41 SURR_L, SURR_R 05h = 101b = Pins 43 & 44 CTR, LFE 06h = 110b = MUTE 07h = 111b = MUTE

9.3.8. Function Select (66h Page 01h)

Register 24h must be set to Page 01h to access this register.

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED			FC3	FC2	FC1	FC0	T/R

Bit(s)	Reset Source	R/W	Reset Value	Name	Description
15-5	n/a	RO	0	RESERVED	BIT NOT USED, SHOULD READ BACK 0
4-1	Reset	RW	00h	FC3:FC0	Function Code bits: 00h - Line Out (Master Out) 01h - Head Phone Out (AUX Out) 02h - DAC 3 (C/LFE) 03h - SPDIF out 04h - Phone In 05h - Mic1 (Mic select =0) 06h - Mic2 (Mic select =1) 07h - Line In 08h - CD In 09h - Video In 0Ah - Aux In 0Bh - Mono Out 0Ch - SPDIF in 0Dh - VREF OUT 0E-0Fh - Reserved For supported Jack and Mic Sense Functions, see Table 22: page 90.The Function Code Bits are used to read Register 68h (Page 01h) and Register 6Ah (Page 01h). Mono I/O should report relevant sense and function information on Tip, and report not supported on Ring. This is true for the following Function codes: 0Bh (Mono Out) and 0Eh (SPDIF Out) Setting the function code to unsupported values will return a 0 when accessing the Information Valid Bit in page 01 register 68h bit 5.
0	Reset	R/W	0	T/R	Tip or Ring selection Bit.This bit sets which jack conductor the sense value is measured from. S/W will program the corresponding the Ring/Tip selector bit together with the I/O number in bits FC[3:0]. 0 - Tip (Left) 1 - Ring (Right)

9.3.9. I/O Misc. (68h, Page 00h)

Register 24h must be set to Page 00h to access this register.

Default: 2001h

D15	D14	D13	D12	D11	D10	D9	D8
NOBLKCHK	SPIS A1	SPIS A0	SPI_SELEN1	SPI_SELEN0	VI	AMute	HP3dB
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
P48 MO	P47 M1	P47 M0	DCS	DBS	DAS	HP SELEN1	HP SELEN0

Bit(s)	Reset Value	R/W	Name	Description
15	0	RW	NOBLKCHK	0 = normal behavior 1 = disable block size checking for spdif_in. This is needed primarily for testing so short blocks can be sent to result in quicker "pll_locked" assertion.
14:13	01	RW	SPISA<1:0>	SPDIF_IN slot select 00= Slots 3/4 01= Slots 7/8 10 = Slots 6/9 11= Slots 10/11
12:11	00	RW	SPI SELEN <1:0>	SPDIF_IN Select and Enable 00= SPDIF Input powered down 01= SPDIF Input to AC LINK 10= SPDIF Input to DAC 2 11= SPDIF Input to both ACLINK and DAC 2
10	0	RW	VI	0 = Respond to SPDIF_IN Valid tag 1 = Ignore SPDIF_IN valid tag
9	0	RW	AMUTE Disable	0= Auto mute when SPDIF stream marked non PCM 1= Auto Mute disabled.
8	0	RW	HP3dB	HEADPHONE +3dB Boost 0= 3dB off 1= 3dB on The values for this bit were reversed on the Rev 0.9 release of the datasheet. Above are the correct values.
7	0	RW	P48 M0	Pin 48 configuration 0= SPDIF OUT 1= ADAT OUT
6:5	00	RW	P47 M1:M0	Pin 47 configuration 00= EAPD output/GPIO 01= No Function 10= SPDIF Input (special buffer for low level signals) 11= SPDIF Input (standard input for high level signals) The values for this bit were reversed on the Rev 0.9 release of the datasheet. Above are the correct values.
4	0	RW	DCS	DAC-C channel Swap 0 = Normal operation 1 = Center and LFE swapped
3	0	RW	DBS	DAC-B channel Swap 0 = Normal operation 1 = Left and Right swapped

Bit(s)	Reset Value	R/W	Name	Description
2	0	RW	DAS	DAC-A channel Swap 0 = Normal operation 1 = Left and Right swapped
1:0	01	RW	HP SELEN <1:0>	Headphone Select and Enable 00b: Pins 35/36 = LINE_OUT Pins 39/41 = LINE_OUT 01b: Pins 35/36 = HEADPHONE_OUT Pins 39/41 = LINE_OUT 10b: Pins 35/36 = LINE_OUT Pins 39/41 = HEADPHONE_OUT 11b: Reserved (undefined, writing this will set it to 00)

9.3.10. Function Information (68h Page 01h)

Register 24h must be set to Page 01h to access this register.

Default: 0010h

D15	D14	D13	D12	D11	D10	D9	D8
G4	G3	G2	G1	G0	INV	DL4	DL3
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
DL2	DL1	DL0	IV	RESERVED			FIP

Bit(s)	R/W	Reset Value	Name	Description
15	RW	see table	G4	Gain Sign Bit: The codec updates this bit with the sign of the gain value present in G[3:0]. The BIOS updates this to take into consideration external amplifiers or other external logic when relevant. G[4] indicates whether the value is a gain or attenuation.
14:11	RW	see table	G3:G0	Gain Bits: The codec updates these bits with the gain value (db relative to level-out) in 1.5dBV increments. The BIOS updates these to take into consideration external amplifiers or other external logic when relevant. G[0:3] indicates the magnitude of the gain. G[4] indicates whether the value is a gain or attenuation. For Gain/Attenuation settings, see Table 21: page 88. These bits are read/write and do not reset on RESET#.
10	RW	see table	INV	Inversion bit: Indicates that the codec presents a 180 degree phase shift to the signal. 0h - No inversion reported 1h - Inverted This bit is read/write and do not reset on RESET#. BIOS should invert for each inverting gain stage.

Bit(s)	R/W	Reset Value	Name	Description
9:5	RW	see table	DL4:DL0	Buffer delays: Codec will provide number a delay measurement for the input and output channels. Software will use this value to accurately calculate audio stream position with respect to what is been reproduced or recorded. These values are in 20.83 microsecond (1/48000 second) units. For output channels, this timing is from the end of AC Link frame in which the sample is provided, until the time the analog signal appears at the output pin. For input streams, this is from when the analog signal is presented at the pin until the representative sample is provided on the AC Link. The measurement is a 'typical' measurement, at a 48KHz sample rate, with minimal in-codec processing (i.e., 3D effects are turned off.) 00h - Information not provided 01h…1Eh - Buffer delay in 20.83usec units 1Fh - reserved These bits are read/write and do not reset on RESET#. The default value is the delay internal to the codec. The BIOS may add to this value the known delays external to the codec, such as for an external amplifier.
4	RW	see table	IV	Information Valid Bit: Indicates whether a sensing method is provided by the codec and if information field is valid. This field is updated by the codec. 0h--After codec RESET# de-assertion, it indicates the codec does NOT provides sensing logic and this bit will be Read Only. After a sense cycle is completed indicates that no information is provided on the sensing method. 1h--After codec RESET# de-assertion, it indicates the codec provides sensing logic for this I/O and this bit is Read/Write. After clearing this bit by writing “1”, when a sense cycle is completed the assertion of this bit indicates that there is valid information in the remaining descriptor bits. Writing “0” to this bit has no effect. BIOS should NOT write this bit, as it is reset on RESET#. See Table 22: page 90 for details on usage of this bit.
3:1	0	0	RESERVED	BIT NOT USED, SHOULD READ BACK 0
0	RO	see table	FIP	Function Information Present This bit is set to a ‘1’ indicates that the G[4:0], INV, DL[4:0](Register 6Ah) are supported and R/W capable. This bit is Read Only.

G[4:0]	Gain or Attenuation (dB relative to level-out)
00000	**0 dBV**
00001	**1.5 dBV**
01111	**24 dBV**
10001	**-1.5 dBV**
11111	**-24 dBV**

Table 21. Gain or Attenuation Examples

9.3.11. Digital Audio Control (6Ah, Page 00h)

To access Register 6Ah, Page 00h must be selected in Register 24h.

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED				HPFOCDIS	SPOR	DO1	RESERVED

Bit(s)	Reset Value	R/W	Name	Description
15:	0	RO	RESERVED	BITS NOT USED, SHOULD READ BACK 0
3	0	RW	HPFOCDIS	High Pass Filter Offset Calculation Disable 0 = Calculation enabled. 1 = Calculation disabled.
2	0	RW	SPOR	Over-ride Register 2Ah, D12 write-lock when spdif_en = 1. All bits except spdif sample-rate are affected (D13-D12). Allows for sub-code changing on-the-fly.
1	0	RW	DO1	**SPDIF Digital Output Source Selection:** DO1 = 0; PCM data from the AC-Link to SPDIF DO1 = 1; ADC record data to SPDIF
0	0	RO	RESERVED	BITS NOT USED, SHOULD READ BACK 0

This read/write register is used to program the SPDIF output status. In the default state, the PCM data path from AC_LINK is enabled and the ADC record inputs are disabled. The DO1 bit controls the input source for the PCM to digital output converters.

9.3.12. Sense Details (6Ah Page 01h)

Register 24h must be set to Page 01h to access this register.

Default: NA

D15	D14	D13	D12	D11	D10	D9	D8
ST2	ST1	ST0	S4	S3	S2	S1	S0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
OR1	OR0	SR5	SR4	SR3	SR2	SR1	SR1

Bit(s)	R/W	Reset Value	Name	Description
15-13	RW	see table	ST2:ST0	Connector/Jack location bits This field describes the location of the jack in the system. 0h - Rear I/O Panel 1h - Front Panel 2h - Motherboard 3h - Dock/External 4h:6h - Reserved 7h - No Connection/unused I/O These bits are Read/Write.
12-8	RO		S4:S0	Sensed bits meaning relates to the I/O being sense as output or inputs. **Sensed bits (outputs): See Table 22: page 90.** This field allows for the reporting of the type of output peripheral/device plugged in the jack. Values specified below should be interrogated in conjunction with the SR[5:0] and OR[1:0] bits for accurate reporting. **Sensed bits (inputs): See Table 22: page 90.** This field allows for the reporting of the type of input peripheral/device plugged in the jack. Values specified below should be interrogated in conjunction with the SR[5:0] and OR[1:0] bits for accurate reporting. This field is Read Only.
7-6	RO		OR1:0	Order Bits. These bits indicate the order the sense result bits SR[5:0] are using. 00 - 10^0 (i.e., Ohms) 01 - 10^1 (i.e., 10 Ohms) 10 - 10^2 (i.e., 100 Ohms) 11 - 10^3 (i.e., 1K Ohms)
5-0	RO		SR5:SR0	Sense Result bits These bits are used to report a vendor specific fingerprint or value. (Resistance, impedance, reactance, ect). This field is Read Only.

Reported Value	Input or Output Peripheral/Device
0h	Data not valid. Indicates that the reported value(s) is invalid.
1h	No connection. Indicates that there are no connected devices.
2h-9h	Not used by STAC9758/59
Ah	Indicates that Sense results are reported as binary values in SR[5:0] and OR[1:0].
Bh-Eh	Reserved
Fh	Not used by STAC9758/59

Table 22. Sensed Bits

9.3.13. Revision Code (6Ch, Page 00h)

To access Register 6Ch, Page 00h must be selected in Register 24h.

Default: xxxxh

D15	D14	D13	D12	D11	D10	D9	D8
MINORREV							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
MAJORREV							

Bit(s)	Reset Value	R/W	Name	Description
15:12	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
11:8	**	RO	MINORREV	Minor Revision ID. These bits are read only and will be updated based on minor device changes which will not require software changes. These bits are un-locked with register 70h (D1:D0 = 11) and will read back all 0's when locked.
7:4	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
3:0	***	RO	MAJORREV	Major Revision ID. These bits are read only and will be updated based on major device changes. These bits are not locked.

9.3.14. DAC Slot Mapping (6Ch, Page 01h)

To access Register 6Ch, Page 01h must be selected in Register 24h.

Default: 3760h

D15	D14	D13	D12	D11	D10	D9	D8
FD3	FD2	FD1	FD0	SD3	SD2	SD1	SD0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
CLD3	CLD2	CLD1	CLD0	RESERVED			

Bit(s)	Reset Value	R/W	Name	Description
15:12		RW	FD[3:0]	DAC-A Slot Mapping (Front) default slots 3&4
11:8		RW	SD[3:0]	DAC-B Slot Mapping (Surround) default slots 7&8
7:4		RW	CLD[3:0]	DAC-C Slot Mapping (Center/LFE) default slots 6&9
3:0	0	RO	RESERVED	RESERVED

9.3.15. Analog Special (6Eh, Page 00h)

To access Register 6Eh, Page 00h must be selected in Register 24h.

Default: 1000h

D15	D14	D13	D12	D11	D10	D9	D8
VREFOUTLVL	VREFOUT DISABLE	MonoOut Mux	AC97MIX	ADC INV	DAC-A INV	DAC-B INV	DAC-CL INV
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
DAC-CR INV	MUTEFIX DISABLE	ADCSLT1	ADCSLT0	HP_APOP DISABLE	MIC GAIN VAL	SPLYOVR EN	SPLYOVR VAL

Bit(s)	Reset Value	R/W	Name	Description
15	0	RW	VREFOUTLVL	VREFOUT voltage adjustment when AVDD=5V 0=VREFOUT voltage is 0.50*avdd 1=VREFOUT voltage is 0.81*avdd Note: When AVDD=3.3V, VREFOUT will be 0.46*avdd regardless of the setting of this bit. The VREFOUTDISABLE bit will override this setting
14	0	RW	VREFOUTDISABLE	0 = VREFOUT voltage available 1 = VREFOUT voltage not available VREFOUT goes high z when this bit is set to 1.
13	0	RW	MonoOut Mux	Mono Out has 3 possible sources. Register 20:D9 (0 = mixer / 1= mic.) If register 20:D9 = 0: *0= mixer 2 output 1= DAC-A output Because of the change in analog architecture and the modification in behavior of reg 20 D15 (POP) this bit is necessary to implement the POP Bypass mode DAC to mono path.
12	1	RW	AC97MIX	0=mixer record contains a mix of all mono and stereo analog input signals, not the DAC (ALL ANALOG mode) 1=mixer record contains a mix of all mono and stereo analog input signals plus the DAC signal (AC97 mode) This bit only has an effect when either Stereo Mix or Mono Mix is selected as the record source in Reg 1Ah. The “ALL ANALOG” mode is used to record all analog sources, perform further processing in the digital domain, including combining with other PCM data, and then route the signal through the DACs directly to the output jacks. A Stereo Mix recording will be affected by the setting of the 3D Effects bit (Reg 20h, Bit D13)
11	0	RW	ADC INV	0=Single bit ADC Data not inverted 1=Single bit ADC Data is inverted
10	0	RW	DAC-A INV	0=Single bit DAC Data 0/1 not inverted 1=Single bit DAC Data 0/1 is inverted
9	0	RW	DAC-B INV	0=Single bit DAC Data 2/3 not inverted 1=Single bit DAC Data 2/3 is inverted
8	0	RW	DAC-CL INV	0=Single bit DAC Data 4 not inverted 1=Single bit DAC Data 4 is inverted
7	0	RW	DAC-CR INV	0=Single bit DAC Data 5 not inverted 1=Single bit DAC Data 5 is inverted

Bit(s)	Reset Value	R/W	Name	Description
6	0	RW	MUTEFIX DISABLE	0 = MUTE FIX Enabled 1 = MUTE FIX Disabled When MUTEFIX_DISABLE = 0, a volume setting of 1Fh on either channel of Reg 02h, Reg 04h, Reg 06h, Reg 36h, or Reg 38h will cause a mute on that channel. This is independent of the other channel. When MUTEFIX_DISABLE = 1, a setting of 1F will cause -46.5dB attenuation on the output. With this setting only the mute bit(s) will cause a mute.
5:4	0	RW	ADCSLT1:0	Select slots for ADC data on ACLINK 00 = left slot 3, right slot 4 01 = left slot 7, right slot 8 10 = left slot 6, right slot 9 11 = left slot 10, right slot 11 This bit field is only active when the MV bit (Reg 6Eh, Page 01, Bit 0) is zero. If the MV bit is set, then this bit field has no effect, and the alternate ADC slot mapping registers in Reg 6Eh, Page 01 are used instead.
3	0	RW	HP_APOP DISABLE	0 = HP APOP Enabled 1 = HP APOP Disabled
2	0	RW	MIC GAIN VAL	Adds +10dB gain to the selected MIC input. Use in conjunction with BOOSTEN (Reg. 0Eh;D6) BOOSTEN MICGAINVAL 0 0 = 0 dB 0 1 = 10 dB 1 0 = 20 dB 1 1 = 30 dB
1	0	RW	SPLYOVR_EN	Supply Override bit allows override of the supply detect. 0=no override on supply detect 1=override supply detect with bit 0
0	0	RW	SPLYOVR_VAL	Supply Override Value provides the analog voltage operation values. 0 = force 3.3v operation 1 = force 5V operation

9.3.16. ADC Slot Mapping (6Eh, Page 01h)

To access Register 6Eh, Page 01h must be selected in Register 24h.

Default: 3000h

D15	D14	D13	D12	D11	D10	D9	D8
LIA3	LIA2	LIA1	LIA0	RESERVED			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED							MV

Bit(s)	Reset Value	R/W	Name	Description
15:12	0011	RW	LIA[3:0]	Mapping of LINE IN ADC, default slots 3&4
11:1	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
0	0	RW	MV	Mapping Valid Bit: indicated that the values programmed into page offsets 6Ch and 6Eh are valid.

9.3.17. SigmaTel Reserved (70h)

9.3.18. Various Functions (72h)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
Line_CE	MIC_CE	SPL1	SPL0	SPARE			Alter Antipop
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
INT APOP	SPLITMUTE	SIFOVRN	SIPER	DPLL_LOCK	SP_RUN	PR_DAC_A	STMICEN

Bit(s)	Reset Value	R/W	Name	Description
15	0	RW	Line_CE	0 = Normal operation 1 = 6dB attenuation to allow 2Vrms at input pin for Consumer Equipment compatibility.
14	0	RW	MIC_CE	0 = Normal operation 1 = 6dB attenuation to allow 2Vrms at input pin for Consumer Equipment compatibility.
13:12	0	RW	SPL[1:0]	Loss of DPLL Lock after 00 = 4 parity errors 01 = 3 parity errors 10 = 2 parity errors 11 = 1 parity errors
11:9	0	RW	SPARE	SPARE
8	0	RW	Alter Antipop	0=power down to VAG 1=power down to GND

Bit(s)	Reset Value	R/W	Name	Description
7	0	RW	INT_APOP	0 = Anti Pop Enabled 1 = Anti Pop Disabled The STAC9758/59 includes an internal power supply anti-pop circuit that prevents audible clicks and pops from being heard when the codec is powered on and off. This function is accomplished by delaying the charge/discharge of the VREF capacitor (Pin 27). C_{VREF} value of 1uF will cause a turn-on delay of roughly 3 seconds, which will allow the power supplies to stabilize before the codec outputs are enabled. The delay will be extended to 30 seconds if a value of C_{VREF} value of 10uF is used. The codec outputs are also kept stable for the same amount of time at power-off to allow the system to be gracefully turned off. The INT_APOP bit allows this delay circuit to be bypassed for rapid production testing. Any external component anti-pop circuit is unaffected by the internal circuit.
6	0	RW	SPLITMUTE	Allows separate mute control bits for Master, Headphone, LineIN, CD, AUX and PCM volume control registers as well as Record Gain register. 0 = Default Value: Left and Right channel mutes are controlled by bit D15 of the respective registers disables writes to all R mute signals and force them to read 0. 1 = Bit D15 of respective register affects only the Left channel Mute and bit D7 affects only the Right Channel Mute enables read and writes to Rmute bit in all Stereo Volume registers. If SPLITMUTE is not set, the bahavior is the same as previous codecs.
5	0	RW	SIFOVRN	SPDIF_IN FIFO OVERRUN STATUS BIT 0=no overrun occurred (defualt) 1=overrun has occurred
4	0	RW	SIPER	SPDIF_IN PARITY ERROR 0=no parity error occurred (defualt) 1=parity error occurred
3	0	RO	DPLL_LOCK	Digital PLL Lock 0= DPLL not locked 1= DPLL locked to SPDIF _IN and data valid
2	0	RO	SP_RUN	SPDIF Running 0= no signal on pin 47 1= signal on pin 47
1	0	RW	PR_DAC_A	Powerdown bit for first DAC 1= powerdown 0= normal operation This is equivalent to PRI, PRJ, and PRK, but applies to the first DAC which is not otherwise accomodated
0	0	RW	STMICEN	Stereo Mic Enable 0= Mono 1= Stereo If this bit is 1, then Reg 20h, D8, causes left/right swap when set to 1.

9.3.19. EAPD Access Register (74h)

Default: 0800h

D15	D14	D13	D12	D11	D10	D9	D8
EAPD	RESERVED			EAPD_OEN	RESERVED		
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED					INTDIS	GPIOACC	GPIOSLT12

Bit(s)	Reset Value	R/W	Name	Description
15	0	RW	EAPD	EAPD Data EAPD data output on EAPD when bit D11 = 1 EAPD data input from pin when bit D11 = 0
14:12	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
11	1	RW	EAPD_OEN	EAPD Pin Ouput Enable 0 = EAPD configured as input pin 1 = EAPD configured as output pin
10:3	0	RO	RESERVED	BIT NOT USED, SHOULD READ BACK 0
2	0	RW	INTDIS	Interrupt disable option. Interrupts cleared by writing a “1” to I4 (Reg24h:D15) 0=will clear both SENSE and GPIO interrupts 1=will only clear SENSE interrupts. GPIO interrupts will have to be cleared in Reg54h.
1	0	RW	GPIOACC	GPIO ACCESS - GPIOs configured as input pass their state to AC link in 1 of two ways: 0= GPIO pin connects directly to AC Link 1= AC Link value reflects Register 54h (sticky, invert, etc applied) This can only be used if a modem codec is not present in the system and using Slot12.
0	0	RW	GPIOSLT12	**For inputs:** 0 = Input state only read from register 54h. AC Link slot 12 returns 0. 1 = input state reflected on AC_Link slot 12. **For outputs:** 0 = GPIO[3:0] pad state is controlled via Reg54h. 1 = GPIO[3:0] pad state is controlled by AC Link slot 12. Register 54h is not updated. This can only be used if a modem codec is not present in the system and using Slot12.

9.3.20. Analog Misc. (76h)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED						JS_MANUAL	JS_STEREO DISABLE

9.3.21. ADAT Control and HPF Bypass (78h)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
ADAT3	ADAT2	ADAT1	ADAT0	RESERVED			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED						DAC SYNC	ADC HPF BYP

Bit(s)	Reset Value	R/W	Name	Description
15:12	0000	RW	ADAT <3:0>	ADAT Lightpipe Control
11:2	0	RO	RESERVED	BITS NOT USED, SHOULD READ BACK 0
1	0	RW	DAC SYNC	Synchronize DACs to channel 0 when at same sample rate 0 = enabled 1 = disables DAC Sync
0	0	RW	ADC HPF BYP	0 = Normal operation, (ADC High Pass Filter active) 1 = ADC High Pass Filter Bypass

9.3.22. SigmaTel Reserved (7Ah)

9.4. Vendor ID1 and ID2 (7Ch and 7Eh)

These two registers contain four 8-bit ID codes. The first three codes have been assigned by Microsoft using their Plug and Play Vendor ID methodology. The fourth code is a SigmaTel, Inc. assigned code identifying the STAC9758/59. The ID1 register (index 7Ch) contains the value 8384h, which is the first (83h) and second (84h) bytes of the Microsoft ID code. The ID2 register (index 7Eh) contains the value 7658h, which is the third (76h) byte of the Microsoft ID code, and 58h which is the STAC9758/59 ID code.

9.4.1. Vendor ID1 (7Ch)

Default: 8384h

D15	D14	D13	D12	D11	D10	D9	D8
1	0	0	0	0	0	1	1
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	0	0	0	0	1	0	0

9.4.2. Vendor ID2 (7Eh)

Default: 7658h

D15	D14	D13	D12	D11	D10	D9	D8
0	1	1	1	0	1	1	0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	1	0	0	0

10. LOW POWER MODES

The STAC9758/59 is capable of operating at reduced power when no activity is required. The state of power down is controlled by the Powerdown Register (26h). There are 7 commands of separate power down. The power down options are listed in Table 23. The first three bits, PR0..PR2, can be used individually or in combination with each other, and control power distribution to the ADC's, DAC's and Mixer. The last analog power control bit, PR3, affects analog bias and reference voltages, and can only be used in combination with PR1, PR2, and PR3. PR3 essentially removes power from all analog sections of the codec, and is generally only asserted when the codec will not be needed for long periods. PR0 and PR1 control the PCM ADC's and DAC's only. PR2 and PR3 do not need to be "set" before a PR4, but PR0 and PR1 should be "set" before PR4. PR5 disables the DSP clock and does not require an external cold reset for recovery. If PR0 and PR1 are set together, it is the same as setting PR5 (like this in the 9756 and 9744). PR6 disables the headphone driver amplifier for additional analog power saving.

GRP Bits	Function
PR0	PCM in ADC's & Input Mux Powerdown
PR1	PCM out DACs Powerdown
PR2	Analog Mixer powerdown (VREF still on)
PR3	Analog Mixer powerdown (VREF off)
PR4	Digital Interface (AC-Link) powerdown (BIT CLK forced low)
PR5	Digital Clk disable, BIT CLK still on
PR6	Powerdown HEADPHONE_OUT

Table 23. Low Power Modes

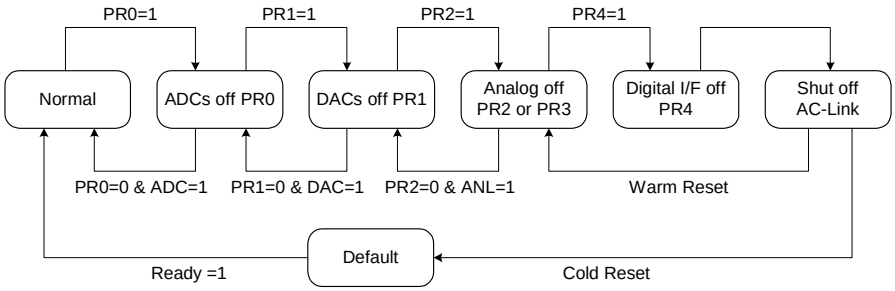


Figure 19. Example of STAC9758/59 Powerdown/Powerup flow

The Figure 19 illustrates one example procedure to do a complete powerdown of STAC9758/59. From normal operation, sequential writes to the Powerdown Register are performed to power down STAC9758/59 a section at a time. After everything has been shut off, a final write (of PR4) can be executed to shut down the AC-Link. The part will remain in sleep mode with all its registers holding their static values. To wake up, the AC'97 controller will send an extended pulse on the sync line, issuing a warm reset. This will restart the AC-Link (resetting PR4 to zero). The STAC9758/59 can also be woken up with a cold reset. A cold reset will reset all of the registers to their default states (Paged Registers are semi-exempt). When a section is powered back on, the Powerdown Control/Status register (index 26h)

should be read to verify that the section is ready (stable) before attempting any operation that requires it.

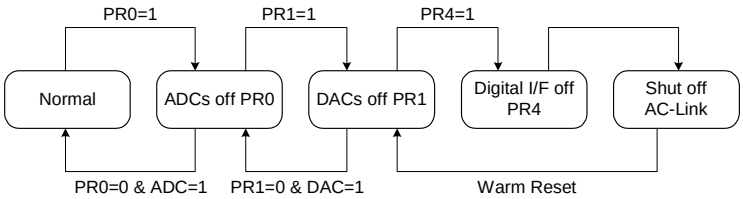


Figure 20. Powerdown/Powerup flow with analog still alive

Figure 20 illustrates a state when all the mixers should work with the static volume settings that are contained in their associated registers. This configuration can be used when playing a CD (or external LINE_IN source) through STAC9758/59 to the speakers, while most of the system in low power mode. The procedure for this follows the previous except that the analog mixer is never shut down.

11. MULTIPLE CODEC SUPPORT

The STAC9758/59 provides support for the multi-codec option according to the Intel AC'97, rev 2.3 specification. The Codec ID functions as a chip select. Secondary devices therefore have completely orthogonal register sets; each is individually accessible and they do not share registers. The STAC9758/59 supports only the Codec ID 10 in secondary mode.

11.1. Primary/Secondary Codec Selection

In a multi-codec environment the codec ID is provided by external programming of pin46 (CID1). The CID pin electrical function is logically inverted from the codec ID designation. The corresponding pin state and its associated codec ID are listed in the "Codec ID Selection" table. Also see slot assignment discussion, “Multi-Channel Programming Register (Index 74)” .

XTAL Out Pin State	CID1 Pin State	CID0 Pin State	Codec ID	Codec Status
GND	Dvdd or floating	NA	00	Primary
XTL/FLOAT	0V	NA	10	Secondary

Table 24. Codec ID Selection

11.1.1. Primary Codec Operation

As a Primary device the STAC9758/59 is completely compatible with existing AC'97 definitions and extensions. Primary Codec registers are accessed exactly as defined in the AC'97 Component Specification and AC'97 Extensions. The STAC9758/59 operates as Primary by default, and the external ID pin (46), has an internal pull-up so that this pin may be left as no-connect for primary operation.

When used as the Primary Codec, the STAC9758/59 generates the master AC-Link BIT_CLK for both the AC'97 Digital Controller and any Secondary Codecs. The STAC9758/59 can support up to four, 10 KW 50 pF loads on the BIT_CLK output. This is to ensure that up to four Codec implementations will not load down the clock output.

11.1.2. Secondary Codec Operation

When the STAC9758/59 is configured as a Secondary device the BIT_CLK pin is configured as an input at power up. Using the BIT_CLK provided by the Primary Codec insures that everything on the AC-Link will be synchronous. As a Secondary device it can be defined as Codec ID 10 only in the two-bit field(s) of the Extended Audio and/or Extended Modem ID Register(s).

11.2. Secondary Codec Register Access Definitions

The AC'97 Digital Controller can independently access Primary and Secondary Codec registers by using a 2-bit Codec ID field (chip select) which is defined as the LSBs of Output Slot 0. For Secondary Codec access, the AC'97 Digital Controller must *invalidate* the tag bits for Slot 1 and 2 Command Address and Data (Slot 0, bits 14 and 13) and place a *non-zero* value (01, 10, or 11) into the Codec ID field (Slot 0, bits 1 and 0).

As a Secondary Codec, the STAC9758/59 will disregard the Command Address and Command Data (Slot 0, bits 14 and 13) tag bits when it sees a 2-bit Codec ID value (Slot 0, bits 1 and 0) that matches its configuration. In a sense the Secondary Codec ID field functions as an alternative Valid Command Address (for Secondary reads and writes) and Command Data (for Secondary writes) tag indicator.

Secondary Codecs must monitor the Frame Valid bit, and ignore the frame (regardless of the state of the Secondary Codec ID bits) if it is not valid. AC'97 Digital Controllers should set the frame valid bit for a frame with a secondary register access, even if no other bits in the output tag slot except the Secondary Codec ID bits are set.

This method is designed to be backward compatible with existing AC'97 controllers and Codecs. There is no change to output Slot 1 or 2 definitions.

Output Tag Slot (16-bits)	
Bit	**Description**
15	Frame Valid
14	Slot 1 Valid Command Address bit (†Primary Codec only)
13	Slot 2 Valid Command Data bit (†Primary Codec only)
12-3	Slot 3-12 Valid bits as defined by AC'97
2	Reserved (Set to “0”)
†1-0	2-bit Codec ID field (00 reserved for Primary; 01, 10, 11 indicate Secondary)

Note: † New definitions for Secondary Codec Register Access

Table 25. Secondary Codec Register Access Slot 0 Bit Definitions

Using three codecs typically requires a controller to support SDATA_IN2.

12. TESTABILITY

The STAC9758/59 has three test modes. One is for ATE in-circuit test and the other two are restricted for SigmaTel's internal use. STAC9758/59 enters the ATE in circuit test mode if SDATA_OUT is sampled high at the trailing edge of RESET#. Once in the ATE test mode, the digital AC-Link outputs (BIT_CLK and SDATA_IN) are driven to a high impedance state. This allows ATE in-circuit testing of the AC'97 controller. Use of the ATE test mode is the recommended means of removing the codec from the AC-Link when another codec is to be used as the primary. This case will never occur during standard operating conditions. Once either of the two test modes have been entered, the STAC9758/59 must be issued another RESET# with all AC-link signals held low to return to the normal operating mode.

SYNC	SDATA_OUT	Description
0	0	Normal AC '97 operation
0	1	ATE Test Mode
1	0	SigmaTel Internal Test Modes
1	1	Reserved

Table 26. Test Mode Activation

12.0.1. ATE Test Mode

ATE test mode allows for in circuit testing to be completed at board level. For this to work, the outputs of the device must be driven to a high impedance state (z). Internal pull-ups and pull-downs for I/O pins are also disabled in this mode. This is the lowest power mode for the device. This mode initiates on the rising edge of RESET# pin. Only a cold reset will exit the ATE Test Mode.

Pin Name	Pin #	Function	Description
SDATA_OUT	5	1	Must be held high at the rising edge of RESET#
BIT_CLK	6	z	high impedance state
SDATA_IN	8	z	high impedance state
SYNC	10	0	Must be held low at rising edge of RESET#
RESET#	11	1	high impedance state
GPIO0	31	z	high impedance state
GPIO1	33	z	high impedance state
GPIO2	34	z	high impedance state
GPIO3	45	z	high impedance state
CID1	46	z	high impedance state
EAPD/SPDIFI	47	z	high impedance state
SPDIFO/ADAT	48	z	high impedance state

Table 27. ATE Test Mode Operation

13. PIN DESCRIPTION

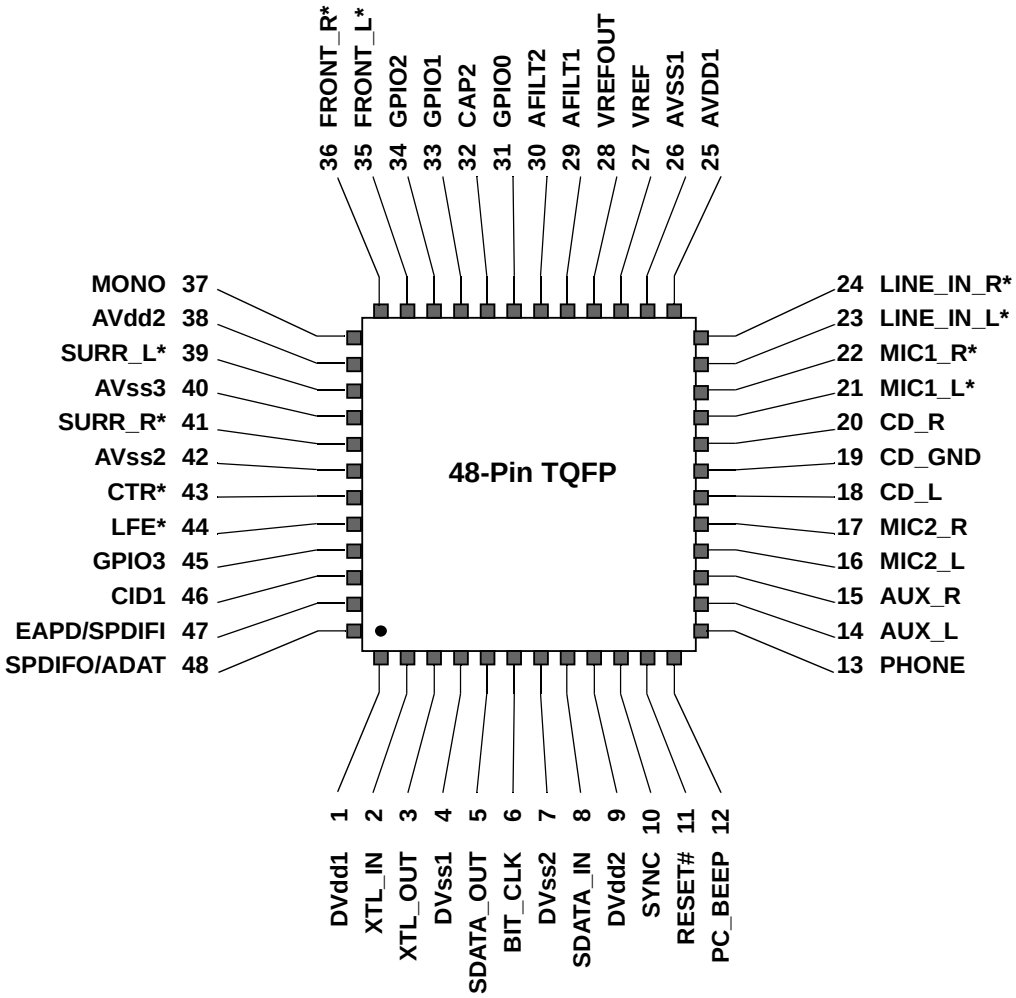


Figure 21. Pin Description Drawing

Note: For use of pins 16/17 for Video, see section 9.0.12: page 57.

Note: If pin 48 is held high at powerup, this bit will be held to zero, to indicate the SPDIF is not available. Tie to ground with a 10K resistor to ensure SPDIF is enabled.

13.1. Digital I/O

These signals connect the STAC9758/59 to its AC'97 controller counterpart, an external crystal, multi-codec selection and external audio amplifier.

Pin Name	Pin #	Type	Description
XTL_IN	2	I	24.576 MHz Crystal or External Clock Source
XTL_OUT	3	I/O	24.576 MHz Crystal
SDATA_OUT	5	I	Serial, time division multiplexed, AC'97 input stream
BIT_CLK	6	I/O	12.288 MHz serial data clock
SDATA_IN	8	O	Serial, time division multiplexed, AC'97 output stream
SYNC	10	I	48 kHz fixed rate sample sync
RESET#	11	I	AC'97 Master H/W Reset
GPIO0	31	I	GPIO tied to AVDD.
GPIO 1	33	I/O	GPIO tied to AVDD.
GPIO 2	34	I/O	GPIO tied to AVDD
GPIO 3	45	I/O	GPIO tied to DVDD
CID1	46	I	Clock input frequency select or Multi-Codec ID select.
EAPD/SPDIFI	47	I/O	External Amplifier Power Down(GPIO)/SPDIF_IN
SPDIFO/ADAT	48	O	SPDIF digital output or ADAT Lightpipe Output NOTE: If pin 48 is held high at powerup, this bit will be held to zero, to indicate the SPDIF is not available. Tie to ground with a 10K resistor to ensure SPDIF is enabled.

Table 28. Digital Connection Signals

13.2. Analog I/O

These signals connect the STAC9758/59 to analog sources and sinks, including microphones and speakers.

Pin Name	Pin #	Type	Description
PC-BEEP	12	I**	PC Speaker beep pass-through
PHONE	13	I**	From telephony subsystem speakerphone
AUX_L	14	I**	Aux Left Channel
AUX_R	15	I**	Aux Right Channel
MIC2_L*	16	I**	Front Panel Mic Left Channel
MIC2_R*	17	I**	Front Panel Mic Right Channel
CD_L	18	I**	CD Audio Left Channel
CD_GND	19	I**	CD Audio analog ground
CD_R	20	I**	CD Audio Right Channel
MIC1_L*	21	I/O*	Desktop Microphone Input
MIC1_R*	22	I/O*	Second Microphone Input
LINE_IN_L*	23	I/O*	Line In Left Channel

Table 29. Analog Connection Signals

Pin Name	Pin #	Type	Description
LINE_IN_R*	24	I/O*	Line In Right Channel
FRONT_L*	35	I/O*	Line Out Left Channel (with headphone support)
FRONT_R*	36	I/O*	Line Out Right Channel (with headphone support)
MONO	37	O	To telephony subsystem speakerphone
SURR_L*	39	I/O*	Surround Out Left Channel (with headphone support)
AVss3	40	I	Headphone Ground Return
SURR_R*	41	I/O*	Surround Out Right Channel (with headphone support)
CTR*	43	I/O*	Center Output
LFE*	44	I/O*	LFE Output

Table 29. Analog Connection Signals

1. ** any unused input pins should be tied together through a capacitor (0.1 µF suggested) to ground, except the MIC inputs which should have their own capacitor to ground if not used.
2. *** Universal Jack**™ capable. These pins may be inputs or outputs and are controlled by registers 64 and 66 (page 0). Only pins 35/36 OR 39/41 may be used to drive headphones. It is not possible to drive 2 sets of headphones at the same time.
3. *For use of pins 16/17 for Video, see section 9.0.12: page 57.*

13.3. Filter/References

These signals are connected to resistors, capacitors, or specific voltages.

Signal Name	Pin Number	Type	Description
VREF	27	O	Analog ground (.45*vdd, at 5V; .41*vdd at 3V)
VREFOUT	28	O	Reference Voltage out 5mA drive (intended for mic bias) (~vdd/2)
AFILT1	29	O	Anti-Aliasing Filter Cap - ADC left channel
AFILT2	30	O	Anti-Aliasing Filter Cap - ADC right channel
CAP2	32	O	ADC reference Cap

Table 30. Filtering and Voltage References

13.4. Power and Ground Signals

Pin Name	Pin #	Type	Description
AVdd1	25	I	Analog Vdd = 5.0V or 3.3V
AVdd2	38	I	Analog Vdd = 5.0V or 3.3V
AVss1	26	I	Analog Gnd
AVss2	42	I	Analog Gnd
AVss3	40	I	analog Gnd
DVdd1	1	I	Digital Vdd = 3.3V
DVdd2	9	I	Digital Vdd = 3.3V
DVss1	4	I	Digital Gnd
DVss2	7	I	Digital Gnd

Table 31. Power and Ground Signals

14. PACKAGE DRAWING

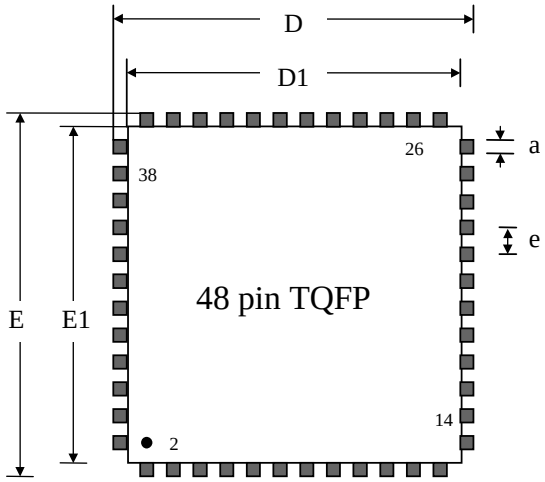


Figure 22. 48-Pin TQFP Package Drawing

Key	TQFP Dimensions
D	9.00 mm
D1	7.00 mm
E	9.00 mm
E1	7.00 mm
a (lead width)	0.20 mm
e (pitch)	0.50 mm
thickness	1.4 mm

Table 32. 48-Pin TQFP Package Dimensions

15. APPENDIX A: PROGRAMMING REGISTERS

Reg #	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	RSRVD	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	6A90h
02h	Master Volume	Mute	RSVD	ML5	ML4	ML3	ML2	ML1	ML0	RMute	RSVD	MR5	MR4	MR3	MR2	MR1	MR0	8000h
04h	DAC-A Volume	Mute	RSVD	HPL5	HPL4	HPL3	HPL2	HPL1	HPL0	RMute	RSVD	HPR5	HPR4	HPR3	HPR2	HPR1	HPR0	8000h
06h	Master Volume Mono	Mute	RESERVED									MM5	MM4	MM3	MM2	MM1	MM0	8000h
0Ah	PC_BEEP Volume	Mute	RSVD	PC_ BEEP_FD	F7	F6	F5	F	F3	F2	F1	F0	PV3	PV2	PV1	PV0	RSRVD	0000h
0Ch	Phone Volume	Mute	RESERVED										GN4	GN3	GN2	GN1	GN0	8008h
0Eh	Mic Volume MONO	ALLMut e	RESERVED		GNL4	GNL3	GNL2	GNL1	GNL0	RMute	BOOST EN	RSRVD	GN4	GN3	GN2	GN1	GN0	8008h
0Eh	MIC Volume STEREO	LMute	RESERVED		GNL4	GNL3	GNL2	GNL1	GNL0	RMute	BOOST EN	RSRVD	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line In Volume	Mute	RESERVED		GL4	GL3	GL2	GL1	GL0	RMute	RESERVED		GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	RESERVED		GL4	GL3	GL2	GL1	GL0	RMute	RESERVED		GR4	GR3	GR2	GR1	GR0	8808h
14h	DAC-B to Mixer2 Volume	Mute	RESERVED		GL4	GL3	GL2	GL1	GL0	RMute	RESERVED		GR4	GR3	GR2	GR1	GR0	8808h
16h	AUX Volume	Mute	RESERVED		GL4	GL3	GL2	GL1	GL0	RMute	RESERVED		GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM Out Volume	Mute	RESERVED		GL4	GL3	GL2	GL1	GL0	RMute	RESERVED		GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Record Select	RESERVED					SL2	SL1	SL0	RESERVED					SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute	RESERVED			GL3	GL2	GL1	GL0	RMute	RESERVED			GR3	GR2	GR1	GR0	8000h
20h	General Purpose	POP	RSRVD	3D	RSVD	DRSS1	DRSS0	MIX	MS	LPBK	RESERVED							0000h
22h	3D Control	RESERVED												DP3	DP2	RESERVED		0000h
24h	Audio Int. & Paging	I4	I3	I2	I1	I0	RESERVED							PG3	PG2	PG1	PG0	0000h
26h	Powerdownn Ctrl/Stat	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	RESERVED				REF	ANL	DAC	ADC	000Fh
28h	Extended Audio ID	ID1	ID0	RESERVED		REV1	REV0	AMAP	LDAC	SDAC	CDAC	DSA1	DSA0	RSVD	SPDIF	DRA	VRA	0BC7
2Ah	Extended Audio Control/ Status	VCFG	PRL	PRK	PRJ	PRI	SPCV	MADC	LDAC	SDAC	CDAC	SPSA1	SPSA0	VRM/ RSVD	SPDIF	DRA	VRA	05F0h
2Ch	PCM DAC Rate (DAC A & DAC-CL	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
2Eh	PCM Surr DAC Rate (DAC-B)	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
30h	PCM LFE DAC Rate (DAC-CR)	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
32h	PCM LR ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
36h	Center/LFE Volume	Mute	RSVD	LFE5	LFE4	LFE3	LFE2	LFE1	LFE0	Mute	RSVD	CNT5	CNT4	CNT3	CNT2	CNT1	CN0	8080h
38h	Surround Volume	Mute	RSVD	LSR5	LSR4	LSR3	LSR2	LSR1	LSR0	Mute	RSVD	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0	8080h
3Ah	SPDIF Control	#V	DRS	SPSR1	SPSR2	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COPY	#PCM/ AUDIO	PRO	2000h
3Eh	Extended Modem Status	RESERVED							PRA	RESERVED							GPIO	0100h
4Ch	GPIO Pin Config	RESERVED												GC3 (GPIO3)	GC2 (GPIO2)	GC1 (GPIO1)	GC0 (GPIO0)	000Fh
4Eh	GPIO Pin Polarity/Type	RESERVED												GP3 (GPIO3)	GP2 (GPIO2)	GP1 (GPIO1)	GP0 (GPIO0)	FFFFh
50h	GPIO Pin Sticky	RESERVED												GS3 (GPIO3)	GS2 (GPIO2)	GS1 (GPIO1)	GS0 (GPIO0)	0000h
52h	GPIO Pin Mask	RESERVED												GW3 (GPIO3)	GW2 (GPIO2)	GW1 (GPIO1)	GW0 (GPIO0)	0000h
54h	GPIO Pin Status	RESERVED												GI3 (GPIO3)	GI2 (GPIO2)	GI1 (GPIO1)	GI0 (GPIO0)	0000h
60h Page 00h	SPDIF_IN Status1	LVL	CC6	CC5	CC4	CC3	CC2	CC1	CC0	MODE1	MODE0	PRE2	PRE1	PRE0	CPY	/AUD	PRO	0000h
60h **Page 01h**	Codec Class/ Rev	X	X	X	CL4	CL3	CL2	CL1	CL0	RV7	RV6	RV5	RV4	RV3	RV2	RV1	RV0	18xxh

Reg #	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
62h Page 00h	SPDIF_IN Status2	SP_VAL	RSVD	CA1	CA0	FS3	FS2	FS1	FS0	CN3	CN2	CN1	CN0	SN3	SN2	SN1	SN0	0000h
62h **Page 01h**	PCI SVID	PVI15	PVI14	PVI13	PVI12	PVI11	PVI10	PVI9	PVI8	PVI7	PVI6	PVI5	PVI4	PVI3	PVI2	PVI1	PVI0	FFFFh
64h Page 00h	Universal Jacks™ Output Select	CSEN	CS1	CS0	RSEN	RS1	RS0	FSEN	FS1	FS0	LS2	LS1	LS0	MSEN	MS1	MS0	RSVD	D794h
64h **Page 01h**	PCI SID	PI15	PI14	PI13	PI12	PI11	PI10	PI9	PI8	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0	FFFFh
66h Page 00h	Universal Jacks™ Input Select	RESERVED					LI2	LI1	LI0	RESERVED					MI2	MI1	MI0	0201h
66h **Page 01h**	Function Select	RESERVED											FC3	FC2	FC1	FC0	T/R	0000h
68h Page 00h	I/O Misc	NOBLK CHK	SPISA1	SPISA0	SPI_SE LEN1	SPI_SE LEN0	VI	AMute	HP3dB	P48MO	p47M1	P47M0	DCS	DBS	DAS	HP_SE LEN1	HP_SE LEN0	2001h
68h **Page 01h**	Function Information	G4	G3	G2	G1	G0	INV	DL4	DL3	DL2	DL1	DL0	IV	RESERVED			FIP	0010h
6Ah Page 00h	Digital Audio Control	RESERVED												HPFOC DIS	SPOR	DO1	RSVD	0000h
6Ah **Page 01h**	Sense Details	ST2	ST1	ST0	S4	S3	S2	S1	S0	OR1	OR0	SR5	SR4	SR3	SR2	SR1	SR0	NA
6Ch	Revision Code																	xxxxh
6Ch **Page 01h**	DAC Slot Mapping	FD3	FD2	FD1	FD0	SD3	SD2	SD1	SD0	CLD3	CLD2	CLD1	CLD0	RESERVED				3760h
6Eh	Analog Special	VREFO UTLVL	VREFO UTDIS ABLE	Mono Out MUX	AC97 ALL MIX	ACD INV	DAC-A INV	DAC-B INV	DAC-CL INV	DAC-CR INV	MUTE FIX DISBLE	ADC slot1	ADC slot0	HP_ APOP DISBLE	MIC GAIN VALUE	SPLY OVR EN	SPLY OVR VAL	1000h
6Eh **Page 01h**	ADC Slot Mapping	LIA3	LIA2	LIA1	LIA0	IMA3	IMA2	IMA1	IMA0	RESERVED							MV	3000h
70h	SigmaTel Reserved	RESERVED																
72h	Various Functions	LINE_C E	MIC_C E	SPL1	SPL0	RSVD			Alter Antipop	INT APOP	SPLIT MUTE	SIF OVRN	SIPER	DPLL_ LOCK	SP_ RUN	PR_ DAC_A	STMIC EN	0000h
74h	EAPD Access	EAPD	RESERVED			EAPD_ OEN	RESERVED								INTDIS	GPIO ACC	GPIO SLT12	0800h
76h	Analog Misc.	RESERVED														JS_MA NUAL	JS-STE REO DISBLE	0000h
78h	ADAT and HPF Bypass	ADAT3	ADAT2	ADAT1	ADAT0	RESERVED										DAC SYNC	ADC HPF BYP	0000h
7Ah	SigmaTel Reserved	RESERVED																
7Ch	Vendor ID1	1	0	0	0	0	0	1	1	1	0	0	0	0	1	0	0	8384h
7Eh	Vendor ID2	0	1	1	1	0	1	1	0	0	1	0	1	1	0	0	0	7658h

16. DOCUMENT CHANGE HISTORY

Change History for Revision 1.0:

Updated power consupmtion numbers
Inserted performance numbers to replace TBDs
Corrected Register 68, Page 0, Bit D8 (HP3dB) inverted values
Corrected Register 68, Page 0, Bit D6:5 values
Corrected type-o error in the Stereo Mic register and SPDIF Reciever referenced in Mixer Diagram
Removed use of BIT_CLK as an input, incorrectly included in the 0.9 release
Corrected secondary mode usage models
Included Video Input usage model section and relevant references
Placed SPDIF Out pin note on connection diagram and pin out
corrected misc grammer, doc flow and type-o's
removed preliminary status