



# C-Media

## Oxygen™ HD CMI8788 High Performance PCI Audio Processor

Data Sheet v0.6



2005/09/12

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## 0. Revision History

| Date       | Rev. | Release Note         |
|------------|------|----------------------|
| 2005/03/15 | 0.1  | Preliminary vision   |
| 2005/04/18 | 0.2  | Modify S/W features  |
| 2005/07/22 | 0.5  | Edit for readability |
| 2005/9/12  | 0.6  | Modify S/W features  |
|            |      |                      |

# 1. Features and General Description

## 1.1 Hardware Features

- PCI 2.2 interface with bus mastering and burst modes
- Only one 24.576MHz oscillator is needed
- 4 synchronous I<sup>2</sup>S output data stream pairs within 1 flexible output DMA
- Programmable channel routing mechanism among the 4 I<sup>2</sup>S output pairs
- 4 synchronous I<sup>2</sup>S input data stream pairs spread in 3 input DMA's (for Dolby pro-audio applications)
- Optionally, a multi-channel AC-link can support 2 AC97 codecs
- Programmable HW monitoring routing from I<sup>2</sup>S inputs to outputs
- All I<sup>2</sup>S I/O pairs support 32-bit PCM data transfer and adjustable sample rate (up to 192KHz)
- Integrated 192k/24-bit S/PDIF transmitter with 1 dedicated S/PDIF OUT DMA
- Integrated 192k/24-bit S/PDIF receiver in recording DMA
- S/PDIF IN supports digital loopback path for switching between optical and RCA connections
- 48k/16-bit front panel DMA for AC97 codec
- 2-wire master serial bus or 4-wire SPI (Serial Peripheral Interface) bus to control I<sup>2</sup>S codecs
- 2-wire slave serial bus to communicate with microcontroller unit (MCU)
- Interrupt pin to inform external MCU to retrieve the data from the system driver
- One MPU-401 MIDI UART port
- EEPROM control interface
- 6 GPI phone jack detection pins
- Advanced device-sensing technology indicates whether a speaker or a headphone is plugged in the jack
- 9 direct-access GPIO pins
- 3 bonding-option bits for 8 identification possibilities
- 128-pin LQFP thin high-quality package

## 1.2 Software Features

- **DTS® Interactive** – a real-time 5.1 channel encoder that takes 2 or more channels and encodes them into a DTS bit stream.
- **DTS® NeoPC** - an up-mix matrix that turns any 2 channel audio into 7.1 channel surround sound
- **Dolby® Digital Live (AC-3)** real-time 5.1 channel encoding bit-stream to facilitate the connection with CE AV receiver
- **Dolby® Pro-Logic IIx** surround processor, spreading stereo audio into 7.1 channel surround sound
- Renowned **Dolby® Headphone** technology, conveying 5.1 surround and 3D gaming audio over stereo headphones
- The latest **Dolby® Virtual Speaker** solution, creating amazing virtual surround sound from a generic two-speaker configuration
- C-Media **FlexBass™** – configurable LFE channel crossover frequency (from 50 to 250Hz)
- C-Media Magic Voice™, a popular feature for disguising voice in online chatting
- C-Media Xear 3D™ 7.1 Virtual Speaker Shifter technology
- C-Media’s unique Karaoke functions: Microphone Echo, Key-shifting
- Individual 10-band EQ for each channel
- 27 global reverberation environments
- Play3D demo program
- Supports most industrial standards of 3D sound for PC gaming, including EAX™ 1.0&2.0, A3D™ 1.0, and DirectSound™
- Support 7.1 CH digital audio playback for WinXP, 2K, ME, 98SE (Microsoft® DirectX V.9.0 and above is required)
- Linux driver available (without Dolby® and DTS® technologies)

## 1.3 General Description

The CMI8788 is a high quality PCI 32-bit multi-channel audio processor that can be built into home audio electronics or personal computers to provide high fidelity sound playback and processing. It supports up to 12 output channels and 8 input channels. The 12 output channels are composed of 3 playback DMA's, which are multi-channel DMA (32 bits, 8 channels, 192k), S/PDIF DMA (32 bits, 2 channels, 192k), and front panel DMA (16 bits, 2 channels, 48k). The 8 input channels are spread across 3 recording DMA's (32 bits, 192k) - recording A, B, and C DMA's. The architecture of recording is a unique point of CMI8788 that enables very flexible recording options for the user. The details of the recording mode selection will be explained in the later sections.

The CMI8788 is compatible with all the popular codecs, from I<sup>2</sup>S codecs with over 120dB quality to the usual AC97 codecs. This ability gives customers the flexibility to design their products exactly the way they want them. The I<sup>2</sup>S, AC-Link, 2-wire master bus, and SPI interfaces are used to transfer audio data and control data between the CMI8788 and codecs. To facilitate the connection with existing home audio electronics, the CMI8788 has incorporated the S/PDIF transmitter and receiver with 192k sampling rate.

An EEPROM interface is built for the CMI8788 in connection with the EEPROM to store and retrieve the non-evaporable data for customer applications, such as board configuration, sub-vendor and sub-system IDs of the PCI configuration, or any dynamic data that customers want to restore at the next power-on.

The CMI8788 has an independent 2-wire slave bus to communicate with the micro control unit (MCU). This interface is used as a medium for the system driver and the MCU to exchange data. One of the applications of the 2-wire slave bus is to transmit the control data from the remote controller to the system driver. The MPU-401 MIDI UART is also integrated in the CMI8788.

There are six GPI phone jack detect pins in CMI8788, which can be used to distinguish if a cable is plugged in the phone jack. There are 9 GPIO pins on the chip, however some of them are shared with other functions. The C-Media's unique device sensing technology is implemented in CMI8788, which can indicate whether a speaker or a headphone is plugged in the jack. Then according to this information, the system driver can decide to turn on the C-Media's X-ear 3D audio technology if appropriate.



## 1.4 Applications

- Prosumer high-quality PCI sound card for retailer market
- Consumer sound card powered by Dolby® and DTS® technologies
- PC-based media center
- Professional PC musician application
- High-end motherboard requiring top audio quality
- Audio up-sell for PC systems
- Bundle selling with high-profile VGA cards
- General purpose multi-channel I/O

## 2. Block Diagram

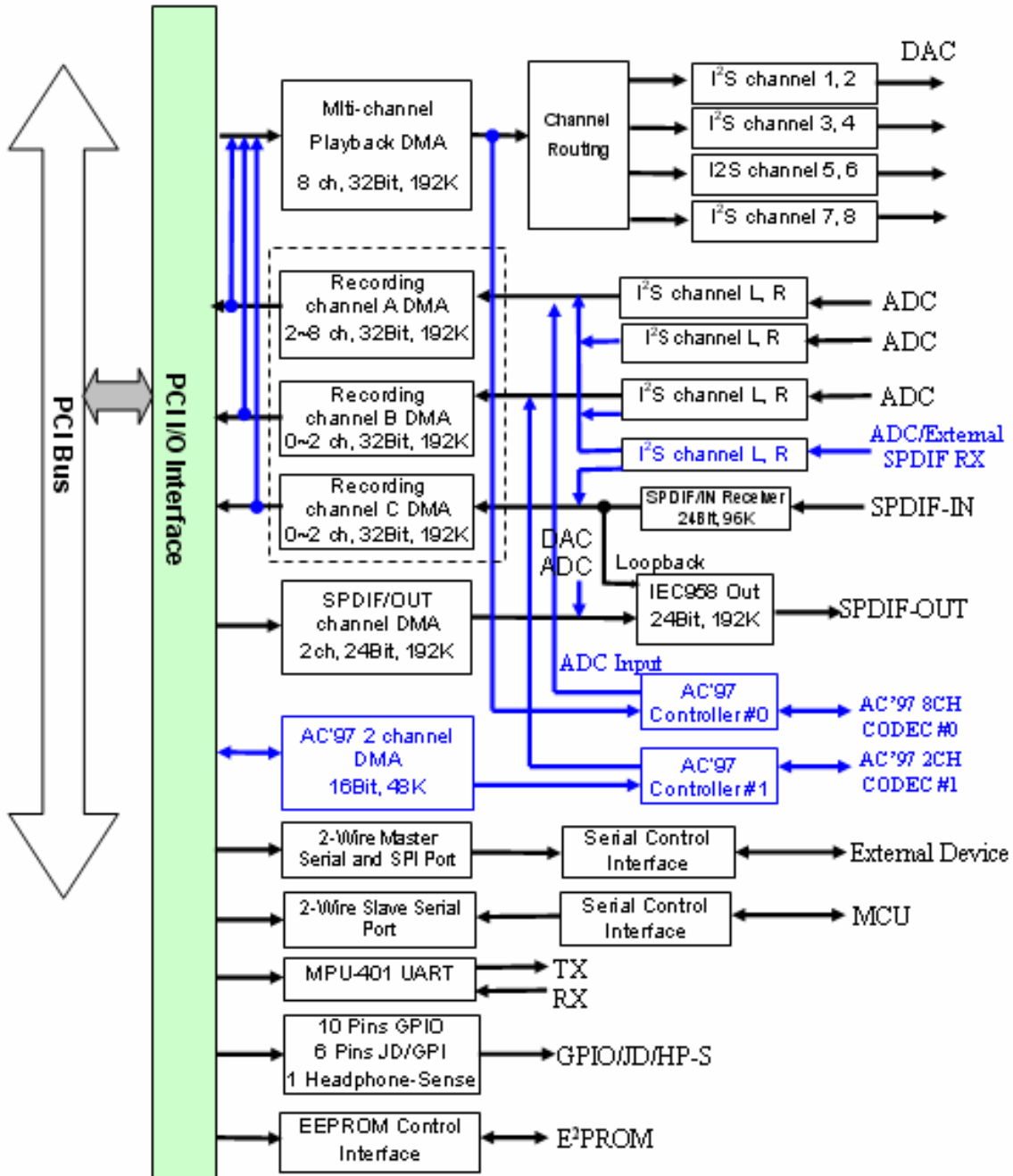


Figure 1. Block Diagram of Oxygen™ HD CMI8788

### 3. Pin Assignment

#### 3.1 Pinout Diagram

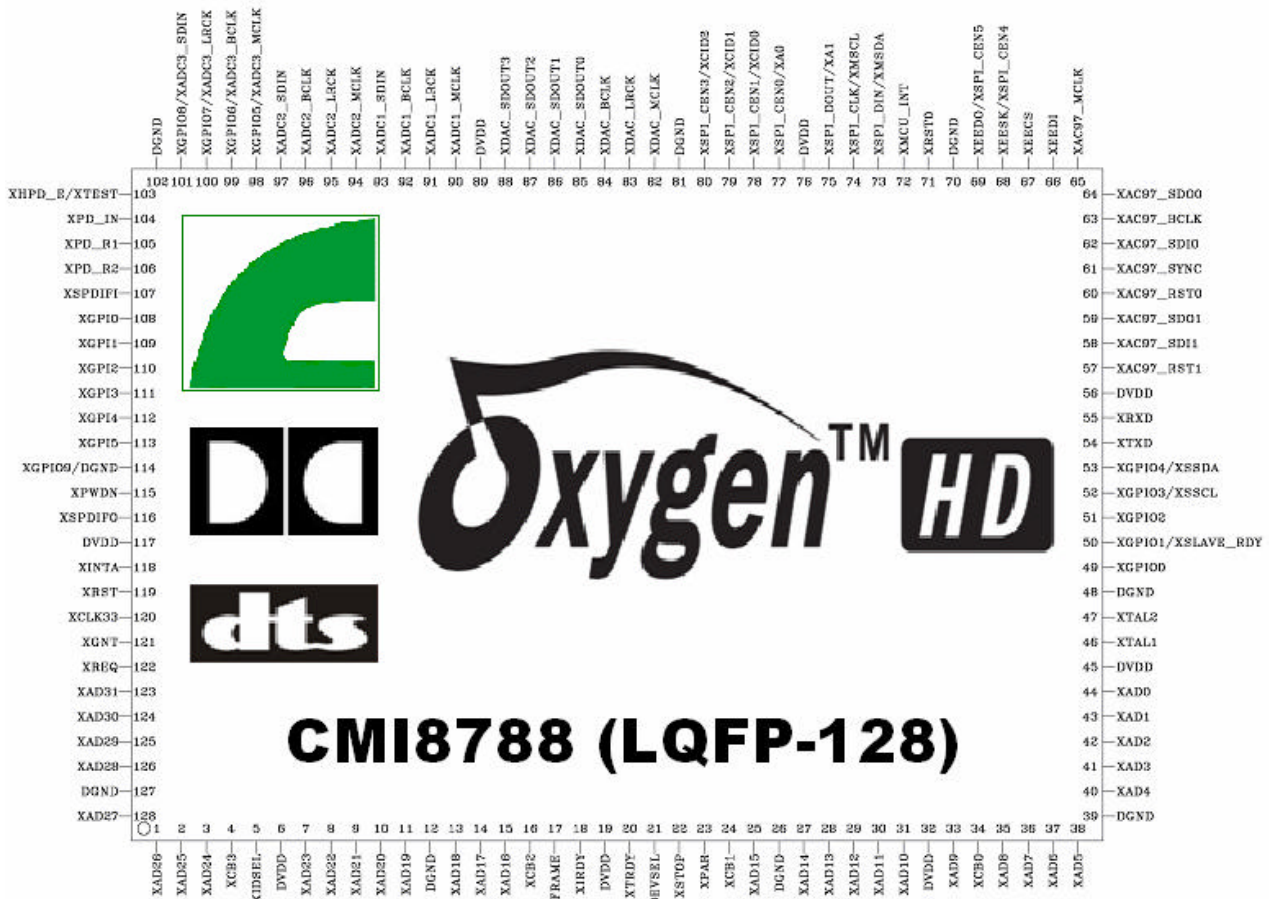


Figure 2. Pinout Diagram of Oxygen™ HD CMI8788

## 3.2 Pin Descriptions

The following table gives the pin descriptions for the Oxygen™HD CMI8788. Some of the pins perform multiple functions, so for the sake of consistency, a pin may be listed more than once in the table. The abbreviations used in the pin description table are explained below.

DI: digital input signal

DO: digital output signal

DIO: digital bidirectional signal

AI: analog input

PU: pull-up with 75K resistor

PD: pull-down with 75K resistor

#: low active signal

**Table 3.1 Pin description table of Oxygen™HD CMI8788**

| Symbol                   | Pin No.   | Type | Description  |
|--------------------------|---|------|--|
| <b>PCI Bus Interface</b> |   |      |  |
| XRST                     | 119   | DI   | PCI Bus Reset.   |
| XCLK33                   | 120   | DI   | PCI Bus clock, 33MHz.  |
| XIDSEL                   | 5   | DI   | PCI Initialization Device Select. This is the chip select during PCI configuration access.                                     |
| XGNT#                    | 121   | DI   | PCI Bus Grant. When active, PCI bus master is granted to CMI8788.  |
| XREQ#                    | 122   | DIO  | PCI Bus Master Request. When active, the CMI8788 is requesting to become a bus master.   |
| XAD[31:0]                | 1-3, 7-11,<br>13-15, 25, 27,<br>28-31, 33,<br>35-38, 40-44,<br>123-126, 128 | DIO  | PCI Address / Data Bus   |
| XCB#[3:0]                | 4, 16, 24, 34   | DIO  | PCI Bus Command / Byte Enable  |
| XFRAME#                  | 17  | DIO  | PCI Cycle Frame. It is driven by the current master to indicate the beginning and duration of an access                        |
| XDEVSEL#                 | 21  | DIO  | PCI Device Select. When active, indicates that the driving device has decoded its address as the target of the current access. |
| XIRDY#                   | 18  | DIO  | PCI Initiator Ready. When active, indicates that the initiator can complete the current data phase of the transaction.         |
| XTRDY#                   | 20  | DIO  | PCI Target Ready. When active, indicates the target device can complete the current data phase of the transaction.             |

|                                    |     |         |  |
|------------------------------------|-----|---------|--|
| XSTOP#                             | 22  | DIO     | PCI Stop. When active, indicates that the target is requesting that the master stop the current transaction.   |
| XPAR                               | 23  | DIO     | PCI Parity. It is even parity across XAD[31:0] and XCB#[3:0].  |
| XINTA#                             | 118 | DIO     | PCI Interrupt Request A.   |
| <b>MPU-401 MIDI UART Interface</b> |     |         |  |
| XTXD                               | 54  | DIO, PU | MP-401 MIDI transmitter (output). It is also used as XGPIO5~8 and I2S ADC 3 configuration (input, 0: GPIO5~8, 1: I2S ADC 3) at the rising edge of XRST.          |
| XRXD                               | 55  | DI, PU  | MPU401 MIDI receiver.  |
| <b>I2S Interface</b>               |     |         |  |
| XDAC_MCLK                          | 82  | DO      | I2S DAC master clock output.   |
| XDAC_LRCK                          | 83  | DIO     | I2S DAC Left/Right sample clock.   |
| XDAC_BCLK                          | 84  | DIO     | I2S DAC bit clock  |
| XDAC_SDOUT0                        | 85  | DO      | I2S DAC channel 0,channel 1 serial data output.  |
| XDAC_SDOUT1                        | 86  | DO      | I2S DAC channel 2,channel 3 serial data output.  |
| XDAC_SDOUT2                        | 87  | DO      | I2S DAC channel 4,channel 5 serial data output.  |
| XDAC_SDOUT3                        | 88  | DO      | I2S DAC channel 6,channel 7 serial data output.  |
| XADC1_MCLK                         | 90  | DO      | I2S ADC 1 and I2S ADC 4 master clock output.   |
| XADC1_LRCK                         | 91  | DIO     | I2S ADC 1 Left/Right sample clock  |
| XADC1_BCLK                         | 92  | DIO     | I2S ADC 1 bit clock.   |
| XADC1_SDIN                         | 93  | DI, PU  | I2S ADC 1 serial data input.   |
| XAC97_SDI1/<br>XADC1_SDIN1         | 58  | DI, PD  | I2S ADC 1 serial data input 1. This pin is shared with AC97 serial data input 1, and determined by XSPI_DOUT/XA1 input configuration at the rising edge of XRST. |
| XADC2_MCLK                         | 94  | DO      | I2S ADC 2 master clock output.   |
| XADC2_LRCK                         | 95  | DIO     | I2S ADC 2 Left/Right sample clock  |
| XADC2_BCLK                         | 96  | DIO     | I2S ADC 2 bit clock.   |
| XADC2_SDIN                         | 97  | DI, PU  | I2S ADC 2 serial data input.   |
| XGPIO5/<br>XADC3_MCLK              | 98  | DIO, PD | I2S ADC 3 master clock output. This pin is shared with XGPIO5, which is determined by XTXD input configuration at the rising edge of XRST.                       |
| XGPIO6/<br>XADC3_BCLK              | 99  | DIO, PD | I2S ADC 3 bit clock. This pin is shared with XGPIO6, which is determined by XTXD input configuration at the rising edge of XRST.                                 |
| XGPIO7/<br>XADC3_LRCK              | 100 | DIO, PD | I2S ADC 2 Left/Right sample clock. This pin is shared with XGPIO7, which is determined by XTXD input configuration at the rising edge of XRST.                   |
| XGPIO8/<br>XADC3_SDIN              | 101 | DIO, PD | GPIO8, default input. This pin is shared with XADC3_SDIN, which determined by XTXD input configuration at the rising edge of XRST.                               |
| <b>AC-Link Interface</b>           |     |         |  |

|                                 |    |         |  |
|---------------------------------|----|---------|--|
| XAC97_BCLK                      | 63 | DI, PU  | AC97 serial clock input8   |
| XAC97_SDI0                      | 62 | DI, PD  | AC97 serial data input 0   |
| XAC97_SDI1/<br>XADC1_SDIN1      | 58 | DI, PD  | AC97 serial data input 1. This pin is shared with XADC1_SDIN1, and determined by XSPI_DOUT/XA1 input configuration at the rising edge of XRST.   |
| XAC97_SYNC                      | 61 | DO      | AC97 frame synchronization.  |
| XAC97_SDO0                      | 64 | DO      | AC97 serial data output 0.   |
| XAC97_SDO1                      | 59 | DO      | AC97 serial data output 1.   |
| XAC97_RST0                      | 60 | DO      | AC97 codec reset 0.  |
| XAC97_RST1                      | 57 | DO      | AC97 codec reset 1.  |
| XAC97_MCLK                      | 65 | DO      | AC97 master clock 24.5760M for AC97 codec.   |
| <b>Serial Port Interface</b>    |    |         |  |
| XSPI_DIN/<br>XMSDA              | 73 | DIO, PU | SPI data input. This pin is shared with 2-wire master serial data.   |
| XSPI_CLK/<br>XMSCL              | 74 | DIO, PU | SPI clock output. This pin is shared with 2-wire master serial clock.  |
| XSPI_DOUT/<br>XA1               | 75 | DIO, PU | SPI data output. This pin is shared with 2-wire Codec address A1. It is also used as XAC97_SDI1 and XADC1_SDIN1 configuration at the rising edge of XRST (input, 1: XAC97_SDI1, 0: XADC1_SDIN1).                           |
| XSPI_CEN0/<br>XA0               | 77 | DIO, PU | SPI chip enable, which select the codec #0 to be controlled. It is shared with I2C Codec address A0. It is also used as XGPIO3~4 and SSCL/SSDA configuration (input, 1: GPIO3~4, 0: SSCL/SSDA) at the rising edge of XRST. |
| XSPI_CEN1/<br>XCID0             | 78 | DIO, PU | SPI chip enable, which select the codec #1 to be controlled (output). It is shared with codec ID 0 configuration (input) at the rising edge of XRST.   |
| XSPI_CEN2/<br>XCID1             | 79 | DIO, PU | SPI chip enable, which select the codec #2 to be controlled (output). It is shared with codec ID 1 configuration (input) at the rising edge of XRST.   |
| XSPI_CEN3/<br>XCID2             | 80 | DIO, PU | SPI chip enable, which select the codec #3 to be controlled (output). It is shared with codec ID 2 configuration (input) at the rising edge of XRST.   |
| XSPI_CEN4/<br>XEESK             | 68 | DO      | SPI chip enable, which select the codec #4 to be controlled. It is shared with EEPROM serial clock.  |
| XSPI_CEN5/<br>XEEDO             | 69 | DO      | SPI chip enable, which select the codec #5 to be controlled. It is shared with EEPROM serial data out.   |
| <b>2-Wire Master Serial Bus</b> |    |         |  |
| XMSDA/<br>XSPI_DIN              | 73 | DIO, PU | 2-wire serial bus data. This pin is shared with SPI data input.  |
| XMSCL/<br>XSPI_CLK              | 74 | DIO, PU | 2-wire serial bus clock. This pin is shared with SPI clock output.   |
| XA1/<br>XSPI_DOUT               | 75 | DIO, PU | 2-wire serial bus codec address A1. This pin is shared with SPI data output. It is also used as XAC97_SDI1 and XADC1_SDIN1 configuration at the rising edge of XRST (input, 1: XAC97_SDI1,                                 |

|                                  |     |         |  |
|----------------------------------|-----|---------|--|
|                                  |     |         | 0: XADC1_SDIN1).   |
| XA0/<br>XSPI_CEN0                | 77  | DIO, PU | 2-wire serial bus codec address A0. This pin is shared with SPI chip enable, which select the codec #0 to be controlled. It is also used as XGPIO3~4 and SSCL/SSDA configuration (input, 1: GPIO3~4, 0: SSCL/SSDA) at the rising edge of XRST. |
| <b>2-Wire Slave Serial Bus</b>   |     |         |  |
| XSSCL/<br>XGPIO3                 | 52  | DIO, PU | 2-wire serial bus clock. This pin is shared with XGPIO3.   |
| XSSDA/<br>XGPIO4                 | 53  | DIO, PU | 2-wire serial bus data. This pin is shared with XGPIO4.  |
| XMCU_INT                         | 72  | DO      | Interrupt output for external Micro Control Unit (MCU).  |
| XSLAVE_RDY/<br>XGPIO1            | 50  | DIO, PD | 2-wire serial bus data ready. This pin is shared with XGPIO1.  |
| <b>S/PDIF Interface</b>          |     |         |  |
| XSPDIFI                          | 107 | DI      | S/PDIF receiver.   |
| XSPDIFO                          | 116 | DO      | S/PDIF transmitter.  |
| <b>EEPROM Interface</b>          |     |         |  |
| XEECS                            | 67  | DIO, PD | EEPROM chip enable (output). It is also used as power on EEPROM CS delay configuration (input, 0: no delay, 1: delay 1 clock) at the rising edge of XRST   |
| XEESK/<br>XSPI_CEN4              | 68  | DO      | EEPROM serial clock. This pin is shared with SPI chip enable, which select the codec #4 to be controlled   |
| XEEDI                            | 66  | DI, PU  | EEPROM serial data in  |
| XEEDO/<br>XSPI_CEN5              | 69  | DO      | EEPROM serial data out. This pin is shared with SPI chip enable, which select the codec #5 to be controlled  |
| <b>Jack Detect GPI Interface</b> |     |         |  |
| XGPIO0                           | 108 | DI, PD  | JACK A detection input   |
| XGPIO1                           | 109 | DI, PD  | JACK B detection input   |
| XGPIO2                           | 110 | DI, PD  | JACK C detection input   |
| XGPIO3                           | 111 | DI, PD  | JACK D detection input   |
| XGPIO4                           | 112 | DI, PD  | JACK E detection input   |
| XGPIO5                           | 113 | DI, PD  | JACK F detection input   |
| <b>GPIO Interface</b>            |     |         |  |
| XGPIO0                           | 49  | DIO, PD | GPIO0, default output Low.   |
| XGPIO1/<br>XSLAVE_RDY            | 50  | DIO, PD | GPIO1, default output Low. This pin is shared with I2C Slave data ready.   |
| XGPIO2                           | 51  | DIO, PD | GPIO2, default input.  |
| XGPIO3/XSSCL                     | 52  | DIO, PU | GPIO3, default output Low. This pin is shared with I2C Slave serial clock.   |
| XGPIO4/XSSDA                     | 53  | DIO, PU | GPIO4, default input. This pin is shared with I2C Slave serial data  |
| XGPIO5/<br>XADC3_MCLK            | 98  | DIO, PD | GPIO5, default output Low. This pin is shared with XADC3_MCLK, which determined by XTXD input configuration  |

|                                    |  |         |   |
|------------------------------------|--|---------|---|
|                                    |  |         | at the rising edge of XRST.   |
| XGPIO6/<br>XADC3_BCLK              | 99                                     | DIO, PD | GPIO6, default input. This pin is shared with XADC3_BCLK, which determined by XTXD input configuration at the rising edge of XRST.      |
| XGPIO7/<br>XADC3_LRCK              | 100                                    | DIO, PD | GPIO7, default output Low. This pin is shared with XADC3_LRCK, which determined by XTXD input configuration at the rising edge of XRST. |
| XGPIO8/<br>XADC3_SDIN              | 101                                    | DIO, PD | GPIO8, default input. This pin is shared with XADC3_SDIN, which determined by XTXD input configuration at the rising edge of XRST.      |
| <b>Headphone Sensing Interface</b> |  |         |   |
| XHPD_E/<br>XTEST                   | 103                                    | DIO, PD | Head phone detect enable. This pin is shared with test mode selection at the rising edge of XRST  |
| XHPD_IN                            | 104                                    | AI      | Head phone voltage input  |
| XHPD_R1                            | 105                                    | AI      | Head phone reference resistor 1   |
| XHPD_R2                            | 106                                    | AI      | Head phone reference resistor 2   |
| <b>Miscellaneous</b>               |  |         |   |
| XTAL1                              | 46                                     | DI      | 24.576Mhz OSC input   |
| XTAL2                              | 47                                     | DO      | OSC output  |
| XRSTO                              | 71                                     | DO      | External Codec reset, can be programmed as Active Low or High with Register 0x50-bit 2  |
| XPWDN                              | 115                                    | DO      | Power Down output pin, Active Low, default High   |
| DVDD                               | 6, 19, 32, 45,<br>56, 76, 89,<br>117   |         | 3.3V power input  |
| DGND                               | 12, 26, 39, 48,<br>70, 81, 102,<br>114 |         | Ground  |



## 4. Electrical Characteristics

### 4.1 Maximum Ratings

#### Test Conditions

DVDD = 3.3V, DGND = 0V, TA = +25°C

| Parameter                     | Symbol | Min | Typ  | Max             | Units |
|-------------------------------|--------|-----|------|-----------------|-------|
| Storage temperature           | -      | -55 | -    | 150             | °C    |
| Operating ambient temperature | -      | 0   | 25   | 75              | °C    |
| DC supply voltage             | -      | 3.0 | 3.3  | 3.6             | V     |
| I/O pin voltage               | -      | GND | -    | V <sub>DD</sub> | V     |
| Power dissipation             | -      | -   | 0.15 | -               | W     |

### 4.2 Recommended Operation Conditions

#### Test Conditions

DVDD = 3.3V, DGND = 0V, TA = +25°C

| Parameter            | Symbol | Min                  | Typ             | Max                  | Units |
|----------------------|--------|----------------------|-----------------|----------------------|-------|
| Input voltage range  | -      | V <sub>DD</sub> -0.3 | V <sub>DD</sub> | V <sub>DD</sub> +0.3 | V     |
| Output voltage range | -      | 0                    | -               | V <sub>DD</sub>      | V     |

### 4.3 Power consumption

#### Test Conditions

DVDD = 3.3V, DGND = 0V, TA = +25°C

| Parameter                   | Symbol | Min | Typ | Max | Units |
|-----------------------------|--------|-----|-----|-----|-------|
| Supply current : power up   | -      | -   | 40  | -   | mA    |
| Supply current : power down | -      | -   | 10  | -   | uA    |

## 4.4 DC Characteristics

### Test Conditions

DVDD = 3.3V, DGND = 0V, TA = +25°C

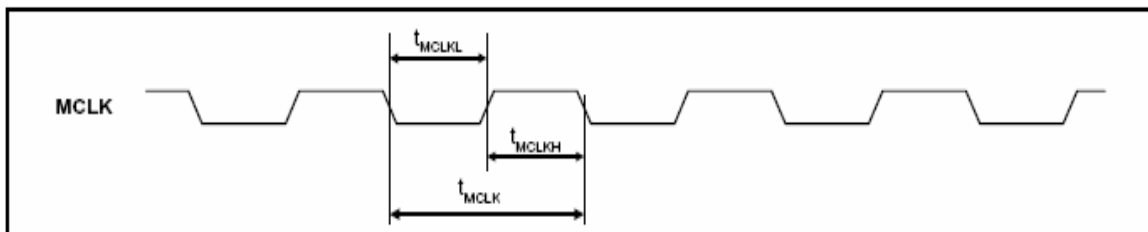
| Parameter                            | Symbol           | Min                  | Typ             | Max                  | Units |
|--------------------------------------|------------------|----------------------|-----------------|----------------------|-------|
| Input voltage range                  | V <sub>in</sub>  | V <sub>DD</sub> -0.3 | V <sub>DD</sub> | V <sub>DD</sub> +0.3 | V     |
| Output voltage range                 | V <sub>out</sub> | 0                    | -               | V <sub>DD</sub>      | V     |
| High level input voltage             | V <sub>ih</sub>  | 0.7V <sub>DD</sub>   | -               | -                    | V     |
| Low level input voltage              | V <sub>il</sub>  | -                    | -               | 0.3V <sub>DD</sub>   | V     |
| High level output voltage            | V <sub>oh</sub>  | 2.4                  | -               | -                    | V     |
| Low level output voltage             | V <sub>ol</sub>  | -                    | -               | 0.4                  | V     |
| Input leakage current                | I <sub>il</sub>  | -10                  | -               | 10                   | uA    |
| Output leakage current               | I <sub>ol</sub>  | -10                  | -               | 10                   | uA    |
| Output buffer driver current         | -                | -                    | 8               | -                    | mA    |
| SPDIF transmit output driver current | -                | -                    | 8               | -                    | mA    |

## 4.5 AC Timing Characteristics

### 4.5.1 I<sup>2</sup>S SIGNAL TIMING

#### 1. SYSTEM CLOCK TIMING

System Clock Timing Diagram



### Test Conditions

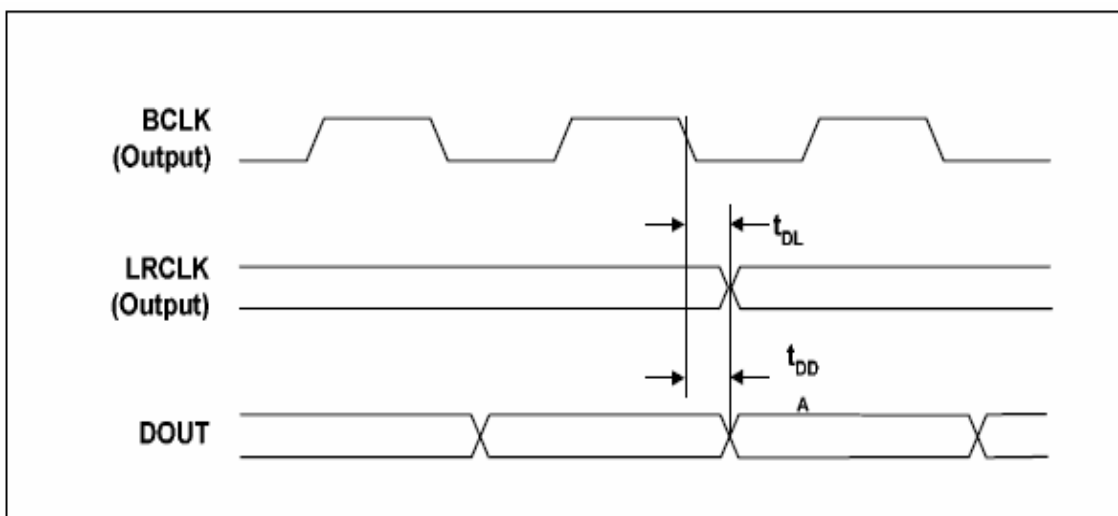
DVDD = 3.3V, DGND = 0V, TA = +25°C, fs = 96KHz, MCLK = 512fs, 24 bit data, unless otherwise stated

System Clock Timing Parameters

| Parameter             | Symbol | Min | Typ | Max | Units |
|-----------------------|--------|-----|-----|-----|-------|
| MCLK clock cycle time | tmclk  | 20  | -   | -   | ns    |
| MCLK pulse width high | tmclkh | 10  | -   | -   | ns    |
| MCLK pulse width low  | tmclkl | 10  | -   | -   | ns    |
| MCLK duty cycle       |        | 40  | 50  | 60  | %     |

## 2. AUDIO INTERFACE TIMING

Audio Interface Timing Diagram



### Test Conditions

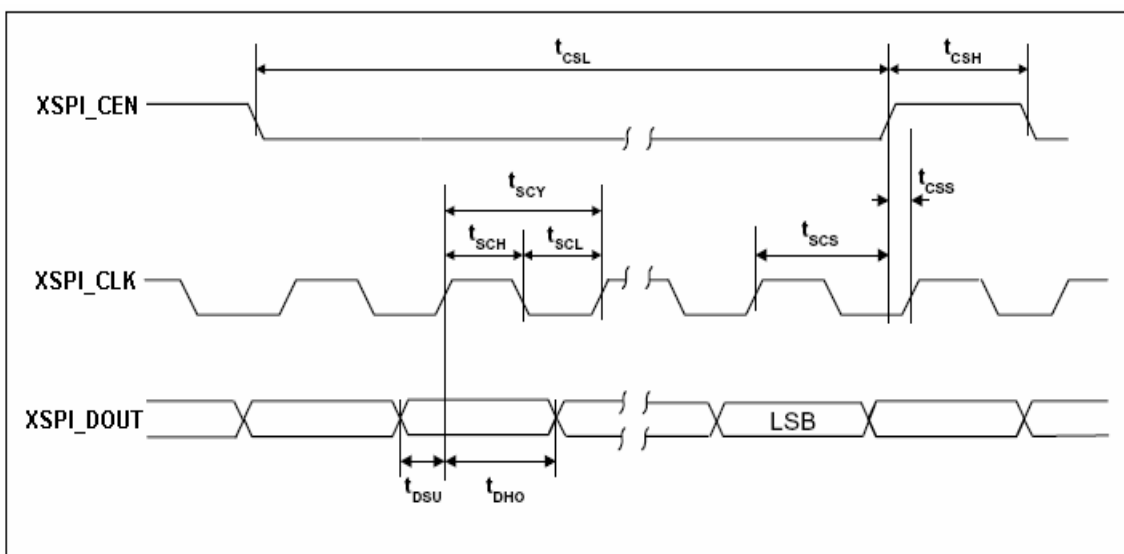
DVDD = 3.3V, DGND = 0V, TA = +25°C, fs = 96KHz, MCLK = 512fs, 24 bit data, unless otherwise stated

Audio Interface Timing Parameters

| Parameter                                      | Symbol | Min | Typ | Max | Units |
|--|--------|-----|-----|-----|-------|
| LRCK propagation delay from BCLK falling edge  | Tdl    | 5   | -   | -   | ns    |
| SDOUT propagation delay from BCLK falling edge | Tdd    | 5   | -   | -   | ns    |

## 4.5.2 CONTROL INTERFACE TIMING - 3 - WIRE MODE

Control Interface Timing -3- Wire Diagram



**Note:** latch data at XSPI\_CEN clock low mode , XSPI\_CEN clock can be low or high mode

### Test Conditions

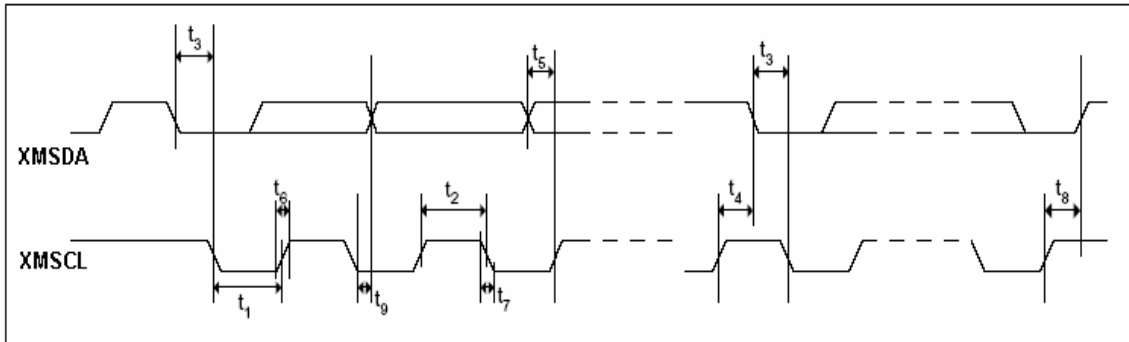
DVDD = 3.3V, DGND =0V, TA=±25°C, SPI clock 160 ns, unless otherwise stated

Control Interface Timing -3- Wire Parameters

| Parameter                                    | Symbol | Min | Typ | Max | Units |
|--|--------|-----|-----|-----|-------|
| XSPI_CLK rising edge to XSPI_CEN rising edge | Tscs   | 120 | -   | -   | ns    |
| XSPI_CLK pulse cycle time                    | Tscy   | 160 | -   | -   | ns    |
| XSPI_CLK pulse width low                     | Tscl   | 80  | -   | -   | ns    |
| XSPI_CLK pulse width high                    | Tsch   | 80  | -   | -   | ns    |
| XSPI_DOUT to XSPI_CLK set-up time            | Tdsu   | 40  | -   | -   | ns    |
| XSPI_DOUT to XSPI_CLK hold time              | Tdho   | 40  | -   | -   | ns    |
| XSPI_CEN rising to SCLK rising               | Tcss   | 40  | -   | -   | ns    |

### 4.5.3 CONTROL INTERFACE TIMING - 2 - WIRE MODE

Control Interface Timing -2- Wire Diagram



**Test Conditions**

DVDD = 3.3V, DGND = 0V, TA = +25°C, 2 wire, Fast speed mode, unless otherwise stated

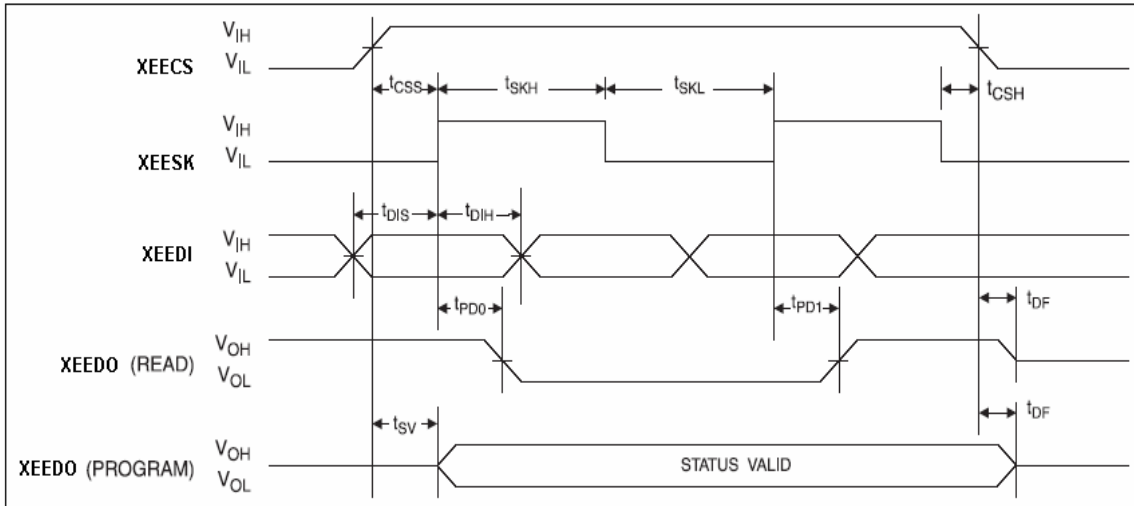
Control Interface Timing -2- Wire Parameters

| Parameter                     | Symbol | Min | Typ | Max | Units |
|-------------------------------|--------|-----|-----|-----|-------|
| XMSCL frequency               |        | 400 | -   | -   | KHz   |
| XMSCL pulse width low         | t1     | 650 | -   | -   | ns    |
| XMSCL pulse width high        | t2     | 1.3 | -   | -   | us    |
| Hold time (start condition)   | t3     | 650 | -   | -   | ns    |
| Set-up time (start condition) | t4     | 650 | -   | -   | ns    |
| Data set-up time              | t5     | 650 | -   | -   | ns    |
| XMSDI, XMSCL rise time        | t6     | 100 | -   | -   | ns    |
| XMSDI, XMSCL fall time        | t7     | 100 | -   | -   | ns    |
| Set-up time (stop condition)  | t8     | 650 | -   | -   | ns    |
| Data hold time                | t9     | 650 | -   | -   | ns    |

**Note:** test parameters at 2 wire, Fast speed mode

## 4.5.4 EEPROM INTERFACE TIMING

**EEPROM Interface Timing Diagram**



### Test Conditions

DVDD = 3.3V, DGND = 0V, TA = +25°C, unless otherwise stated

**EEPROM Interface Timing Parameters**

| Parameter                        | Symbol | Min | Typ | Max | Units |
|----------------------------------|--------|-----|-----|-----|-------|
| XEESK clock frequency            | tsk    | 555 | -   | -   | KHz   |
| XEESK high time                  | tskh   | 900 | -   | -   | ns    |
| XEESK low time                   | tskl   | 900 | -   | -   | ns    |
| XEECS setup time                 | tcss   | 900 | -   | -   | ns    |
| XEEDI setup time                 | tdis   | 900 | -   | -   | ns    |
| XEECS hold time                  | tcsH   | 900 | -   | -   | ns    |
| XEEDI hold time                  | tdih   | 2   | -   | -   | ns    |
| Output delay to "1"              | tpd1   | 900 | -   | -   | ns    |
| Output delay to "0"              | tpd0   | 30  | -   | -   | ns    |
| XEECS to status valid            | tsv    | 30  | -   | -   | ns    |
| XEECS to XEEDO in high impedance | tdf    | 30  | -   | -   | ns    |

#### 4.5.5 EEPROM AC Timing Characteristics

| Symbol      | Description             | Min | Max | Units |
|-------------|-------------------------|-----|-----|-------|
| <b>fsk</b>  | SK Clock Frequency      | 0   | 0.5 | MHz   |
| <b>tskh</b> | SK High Time            | 500 |     | ns    |
| <b>tskl</b> | SK Low Time             | 500 |     | ns    |
| <b>tcss</b> | CS Setup Time           | 100 |     | ns    |
| <b>tcsH</b> | CS Hold Time            | 0   |     | ns    |
| <b>tdis</b> | DI Setup Time           | 200 |     | ns    |
| <b>tdih</b> | DI Hold Time            | 200 |     | ns    |
| <b>tpd0</b> | Output Delay to “0”     |     | 500 | ns    |
| <b>tpd1</b> | Output Delay to “1”     |     | 500 | ns    |
| <b>tsv</b>  | CS to Status Valid      |     | 500 | ns    |
| <b>tdf</b>  | CS to DO High Impedance |     | 200 | ns    |

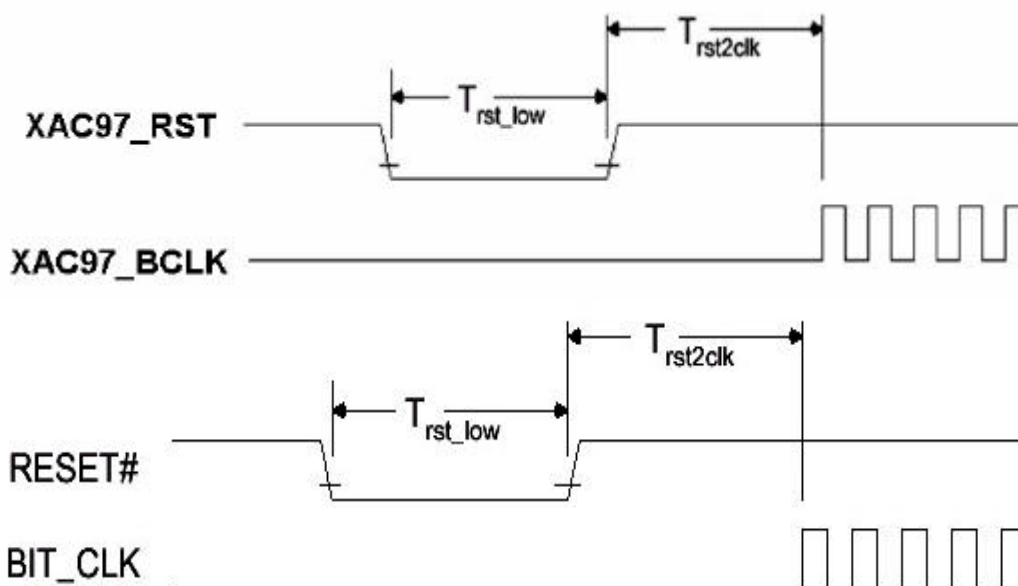
## 4.5.6 AC-LINK TIMING CHARACTERISTICS

### Test Conditions

DVDD = 3.3V, DGND = 0V, TA = +25°C, unless otherwise stated

### 1. COLD RESET

Cold Reset Timing Diagram



Cold Reset Timing Parameters

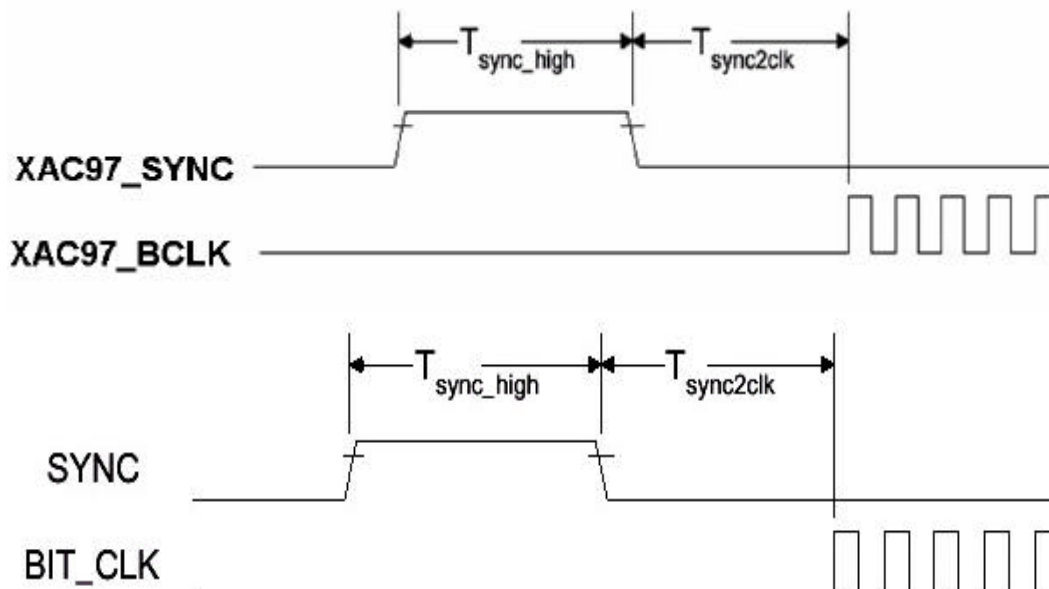
| Parameter                                      | Symbol         | Min | Typ | Max | Units |
|--|----------------|-----|-----|-----|-------|
| XAC97_RST active low pulse width               | $T_{rst\_low}$ | 1.7 | -   | -   | us    |
| XAC97_RST inactive to XAC97_BCLK startup delay | $T_{rst2clk}$  | 168 | -   | -   | ns    |

# denotes active low.



## 2. WARM RESET

Warm Reset Diagram

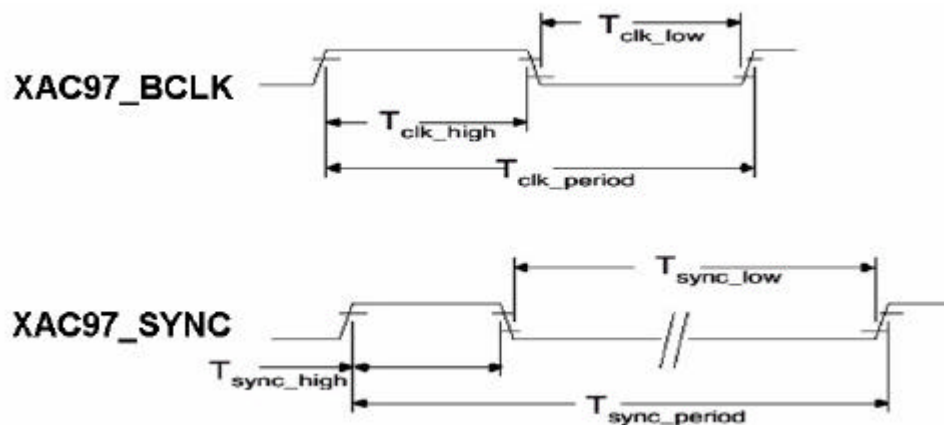


Warm Reset Parameters

| Parameter                                       | Symbol           | Min | Typ | Max | Units |
|---|------------------|-----|-----|-----|-------|
| XAC97_SYNC active high pulse width              | $T_{sync\_high}$ | 1.2 | -   | -   | us    |
| XAC97_SYNC inactive to XAC97_BCLK startup delay | $T_{sync2clk}$   | 168 | -   | -   | ns    |

## 3. AC-LINK CLOCKS

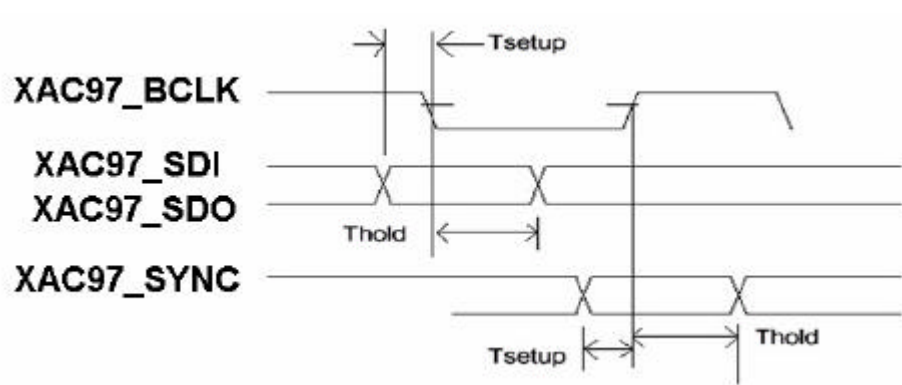
BIT\_CLK to SYNC Timing Diagram



**BIT\_CLK to SYNC Timing Parameters**

| Parameter                           | Symbol       | Min    | Typ | Max | Units |
|-------------------------------------|--------------|--------|-----|-----|-------|
| XAC97_BCLK frequency                |              | 12.288 | -   | -   | MHz   |
| XAC97_BCLK period                   | Tclk_period  | 81.4   | -   | -   | ns    |
| XAC97_BCLK output jitter            |              | 750    | -   | -   | ps    |
| XAC97_BCLK high pulsewidth (note 1) | Tclk_high    | 40.7   | -   | -   | ns    |
| XAC97_BCLK low pulse width (note 1) | Tclk_low     | 40.7   | -   | -   | ns    |
| XAC97_SYNC frequency                |              | 48.0   | -   | -   | kHz   |
| XAC97_SYNC period                   | Tsync_period | 20.8   | -   | -   | us    |
| XAC97_SYNC high pulse width         | Tsync_high   | 1.3    | -   | -   | us    |
| XAC97_SYNC low_pulse width          | Tsync_low    | 19.5   | -   | -   | us    |

**Note:** Worst case duty cycle restricted to 45/55.

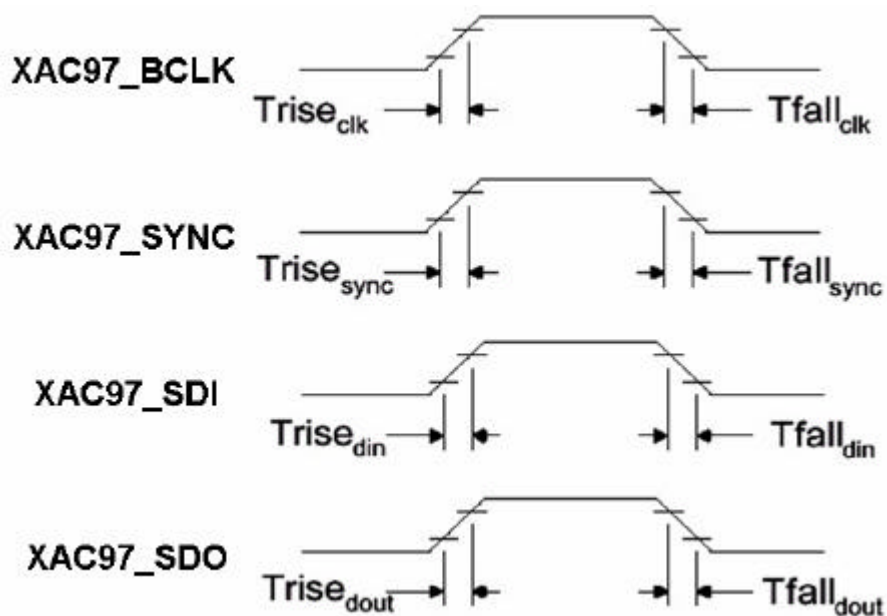
**4. DATA SETUP AND HOLD**
**Data Setup and Hold diagram**

**Data Setup and Hold Parameters**

| Parameter                            | Symbol | Min | Typ | Max | Units |
|--------------------------------------|--------|-----|-----|-----|-------|
| Setup to falling edge of XAC97_BCLK  | Tsetup | 30  | -   | -   | ns    |
| Hold from falling edge of XAC97_BCLK | Thold  | 30  | -   | -   | ns    |

**Note:** Setup and hold time parameters for SDATA\_IN are with respect to the AC '97 Controller.

## 5. SIGNAL RISING AND FALLING TIMES

Signal Rising and Falling Times Diagram

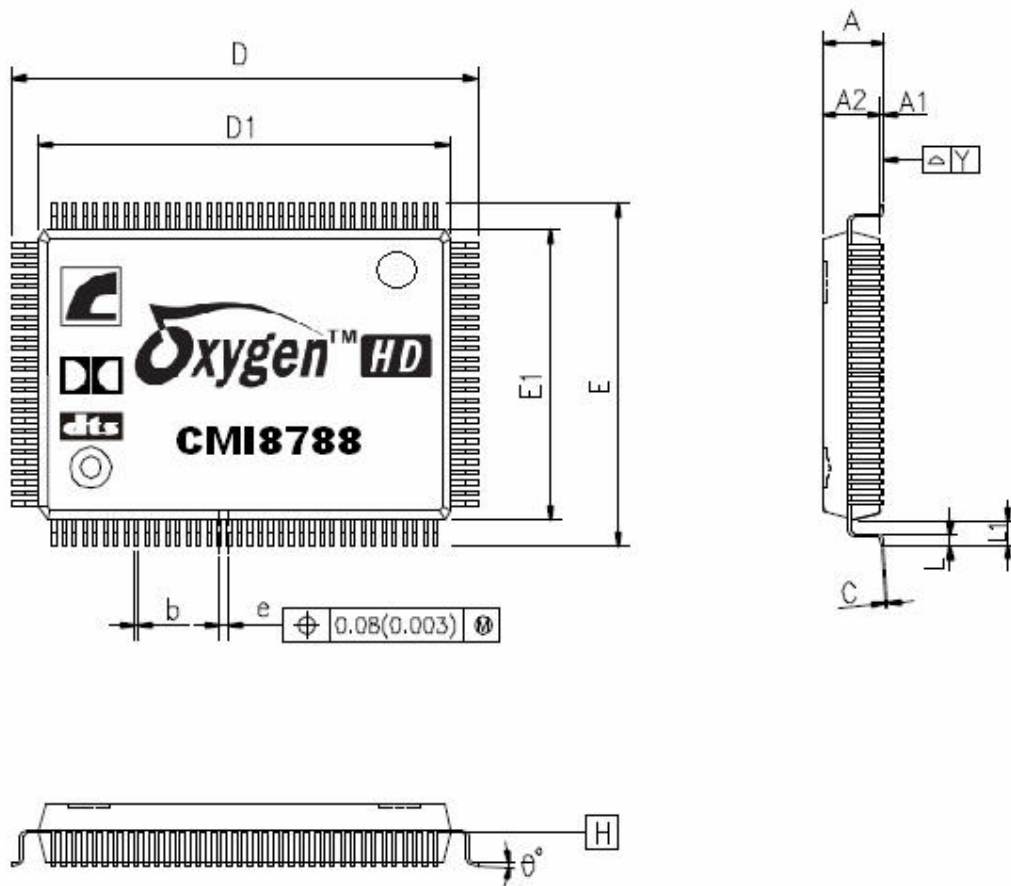


Signal Rising and Falling time Parameters

| Parameter               | Symbol            | Min | Typ | Max | Units |
|-------------------------|-------------------|-----|-----|-----|-------|
| XAC97_BCLK rising time  | $T_{rise_{clk}}$  | 6   | -   | -   | ns    |
| XAC97_BCLK falling time | $T_{fall_{clk}}$  | 6   | -   | -   | ns    |
| XAC97_SYNC rising time  | $T_{rise_{sync}}$ | 6   | -   | -   | ns    |
| XAC97_SYNC falling time | $T_{fall_{sync}}$ | 6   | -   | -   | ns    |
| XAC97_SDI rising time   | $T_{rise_{din}}$  | 6   | -   | -   | ns    |
| XAC97_SDI falling time  | $T_{fall_{din}}$  | 6   | -   | -   | ns    |
| XAC97_SDO rising time   | $T_{rise_{dout}}$ | 6   | -   | -   | ns    |
| XAC97_SDO falling time  | $T_{fall_{dout}}$ | 6   | -   | -   | ns    |

## 5. Mechanical Specification

### 5.1 Package Dimension



| SYMBOLS        | MIN. | NOM.      | MAX. |
|----------------|------|-----------|------|
| A              | -    | -         | 1.60 |
| A1             | 0.05 | -         | 0.15 |
| A2             | 1.35 | 1.40      | 1.45 |
| b              | 0.17 | 0.22      | 0.27 |
| c              | 0.10 | 0.15      | 0.20 |
| D1             | -    | 20.00 BSC | -    |
| E1             | -    | 14.00 BSC | -    |
| e              | -    | 0.50 BSC  | -    |
| D              | -    | 22.00 BSC | -    |
| E              | -    | 16.00 BSC | -    |
| L              | 0.45 | 0.60      | 0.75 |
| L1             | -    | 1.00 REF  | -    |
| Y              | -    | -         | 0.08 |
| $\theta^\circ$ | 0°   | 3.5°      | 7°   |

UNIT : mm

#### NOTES.

- JEDEC OUTLINE.MS-026 BHB
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DIMENSIONS E1 AND D1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS E AND E DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

**- End of Datasheet -**

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