



ChangAn Music Synthesizer Chip Fact Sheet

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Other patents pending.

Released by Creative Advanced Technology Center

Revision History

Date	Revision
April 15, 2005	1.0

Topics

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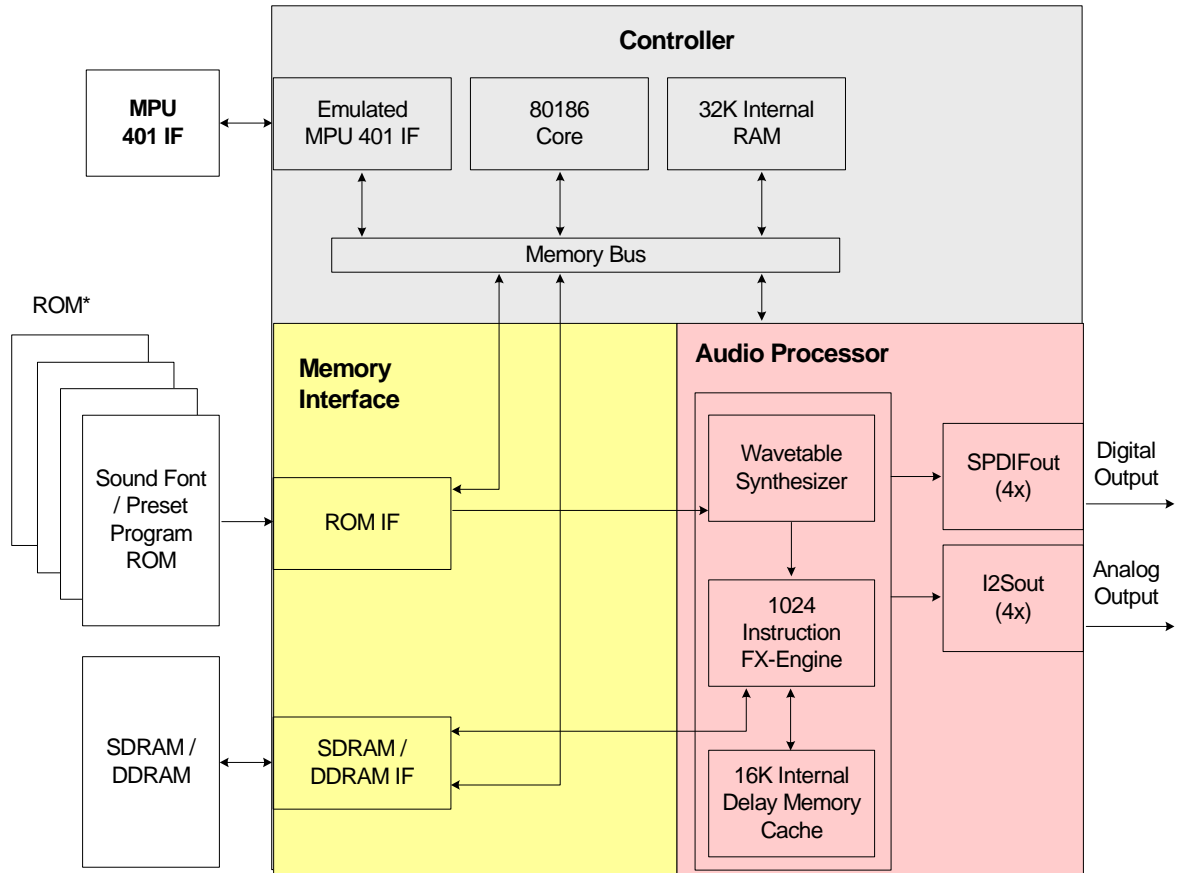
General Description

Creative's ChangAn Music Synthesizer chip is a high quality, standalone music synthesis solution providing 128 channels of wavetable synthesis with integrated effects, microcontroller, MPU401 interface, and industry standard serial interface.

Hardware Feature Summary

- Supports up to 128 Mbyte sound font memory for wavetable synthesis using FLASH ROM memory
- Audio processor with 128-channel 16 or 24 bit wavetable synthesis and effects processing
- Supports up to 2 Mbyte external delay line memory using SDRAM/DDRAM
- 4 stereo 24-bit I2S outputs operating at programmable output rate of 48 or 96 kHz sample rate
- 4 stereo 24-bit S/PDIF outputs operating at programmable output rate of 48 or 96 kHz sample rate
- 2 input serial MIDI UART ports
- 2 output serial MIDI UART ports
- 1 emulated MPU-401 parallel UART port
- 1 I2C interface
- 1 SPI Interface
- 80186 Controller with 32K internal scratch memory

ChangAn Internal Architecture



Feature Details

Controller Sub-Module

The Controller sub-module contains:

- 80186 V micro-controller
- Emulated MPU401 IF (port)
- 32 kByte internal “scratch pad” RAM

□ V80186 Micro-Controller Core

The micro-controller implements the MIDI interpreter. When 80186 controller receives a valid MIDI command via the MPU401 or any of the serial MIDI ports, it translates the command and programs the audio processor wavetable core to play a note.

□ Emulated MPU401 Port

The emulated MPU401 port has two functions:

- MPU401 port
- General purpose IO access of audio processor internal registers via V80186 controller.
- Direct Flash IO

The external host controller can access EMU10k2.5 registers via the V80186 controller. This allows the user to adjust preprogrammed audio effects.

Memory Interface

The ChangAn memory management unit contains a FLASH ROM interface and a SDRAM interface. The FLASH interface is used to fetch

- Firmware code and preset values required by 80186 controller,
- Sound Font sample required by EMU10k2.5 core for Wavetable synthesis.
- Pre-fill the sound channel cache.

ChangAn FLASH ROM interface supports the Samsung and Toshiba FLASH NOR ROM interface.

The current FLASH ROM size available is 32 Mbyte and up to 4 such ROM can be mounted to the chip to implement a 128 Mbyte sound font.

The SDRAM/DDRAM is used to implement long tank delays line required by effects processor core. The SDRAM interface transfers data sample to and from external SDDRAM. It will also initialize and refresh the SDRAM at regular intervals.

Audio Processor

The Audio Processor contains two main modules:

- 128 channel wavetable synthesis sound engine
- Effects engine

When programmed by the controller to synthesize a MIDI note, the programmed wavetable synthesis channel picks up a sound sample from the sound font data bank, and applies the required envelope, pitch control and volume setting to synthesize the correct MIDI note.

These sound channels are routed to the effects processor for mixing. The effects processor also applies audio effects as required by application before the processor routes the audio to the outputs.

I/O Interface

The total estimated pin out is 128: 108 function pins and 20 pins for power supply.

Pin Description

Signal	Number	Type	Type,Drvie	Max Vin	Special	Description
Test	1	IN	TTL	5 V	PD	Test mode pin
Reset	1	IN	TTL	5 V	PU	Chip reset
xtal_in	1	IN				Crystal clock in
xtal_out	1	OUT				Crystal clock in
sdram_clk	1	OUT	CMOS,4mA			SDRAM clock
sdram_fb_clk	1	IN	TTL		PD	SDRAM feedback clock
sdram_chip_sel	1	OUT	CMOS,4mA			SDRAM chip select
sdram_bank_addr	2	OUT	CMOS,4mA			SDRAM access of up to 1 M address byte location.
sdram_addr	12	OUT	CMOS,4mA			SDRAM access of up to 1 M address byte location.
sdram_dat	16	BI	CMOS,4mA	3.3 V		SDRAM data
sdram_ras	1	OUT	CMOS,4mA			SDRAM row access select
sdram_cas	1	OUT	CMOS,4mA			SDRAM column access select
sdram_we	1	OUT	CMOS,4mA			SDRAM write enable
flash_type_sel	1	IN	TTL		PD	FLASH ROM type
flash_size_sel	2	IN	TTL		PD	FLASH ROM size
flash_ctl_ad	34	OUT	CMOS,4mA			FLASH ROM control
flash_dq	16	BI	CMOS,4mA			FLASH ROM data
flash_we	1	OUT	CMOS,4mA			FLASH ROM ready
flash_rdy	1	IN	TTL		PU	FLASH ROM ready
spdifout	4	BI	CMOS,8mA			Spdif output
i2s_out_lrclk	1	OUT	CMOS,4mA			I2s output LR clock
i2s_out_bclk	1	OUT	CMOS,4mA			I2s output bit clock
i2s_out_mclk	1	OUT	CMOS,4mA			I2s output chip clock
i2s_out	4	OUT	CMOS,4mA			I2s output data
i2s_in	1	IN	TTL		PD	I2s input data
inMidi	2	IN	TTL	5V	ST,PU,FS	INMIDI
outMidi	2	OUT	CMOS,8mA			OUTMIDI
mpu401_csn	1	IN	TTL	5 V	PU	MPU chip select
mpu401_addr	4	IN	TTL	5 V	PU	MPU address.
mpu401_rdn	1	IN	TTL	5 V	PU	MPU read
mpu401_wrn	1	IN	TTL	5 V	PU	MPU write
mpu401_data	8	BI	CMOS,4mA			MPU data
gpio	8	BI	CMOS,4mA	5 V		
spi_scs	1	OUT	CMOS,4mA			
spi_sclk	1	OUT	CMOS,4mA			
Spi_sdo	1	OUT	CMOS,4mA			

Signal	Number	Type	Type,Drvie	Max Vin	Special	Description
i2c_scl	1	BI	CMOS,4mA			
i2c_sda	1	BI	CMOS,4mA			
VDD_CORE	TDB	PWR	-	-	-	Chip core Power (?? V) +/- 10 %
VSS_CORE	TDB	PWR	-	-	-	Chip Ground
VDD_IO	TDB	PWR	-	-	-	IO Power (3.3 V) +/- 10 %
VSS_IO	TDB	PWR	-	-	-	IO Ground
VDDA_PLL	TDB	PWR	-	-	-	Analog PLL Power (??V) +/- 10 %
VSSA_PLL	TDB	PWR	-	-	-	Analog Ground

Pin Location

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	flash_ctl_ad_33	45	flash_dq_15	89	sdram_chip_sel	133	inMidiA
2	flash_ctl_ad_32	46	flash_dq_14	90	sdram_ras	134	inMidiB
3	flash_ctl_ad_31	47	flash_dq_13	91	sdram_cas	135	
4	flash_ctl_ad_30	48	flash_dq_12	92	sdram_we	136	OutMidiA
5	flash_ctl_ad_29	49	flash_dq_11	93		137	OutMidiB
6		50		94	sdram_bank_addr_1	138	
7	flash_ctl_ad_28	51	flash_dq_10	95	sdram_bank_addr_0	139	gpio7
8	flash_ctl_ad_27	52	flash_dq_9	96		140	gpio6
9	flash_ctl_ad_26	53	flash_dq_8	97	sdram_addr_11	141	gpio5
10	flash_ctl_ad_25	54	flash_dq_7	98	sdram_addr_10	142	gpio4
11	flash_ctl_ad_24	55	flash_dq_6	99	sdram_addr_9	143	gpio3
12		56		100	sdram_addr_8	144	
13	flash_ctl_ad_23	57	flash_dq_5	101	sdram_addr_7	145	gpio2
14	flash_ctl_ad_22	58	flash_dq_4	102		146	gpio1
15	flash_ctl_ad_21	59	flash_dq_3	103	sdram_addr_6	147	gpio0
16	flash_ctl_ad_20	60	flash_dq_2	104	sdram_addr_5	148	
17	flash_ctl_ad_19	61	flash_dq_1	105	sdram_addr_4	149	
18		62	flash_dq_0	106	sdram_addr_3	150	Test
19	flash_ctl_ad_18	63		107	sdram_addr_2	151	PLLVDDB
20	flash_ctl_ad_17	64	flash_type_sel	108	sdram_addr_1	152	xtalin
21	flash_ctl_ad_16	65	flash_size_sel_0	109	sdram_addr_0	153	Xtalout
22	flash_ctl_ad_15	66	flash_size_1	110		154	PLLVSS
23	flash_ctl_ad_14	67		111	sdram_clk	155	
24		68	mpu401_csn	112	sdram_fb_clk	156	i2c_sda
25	flash_ctl_ad_13	69	mpu401_rdn	113		157	i2c_scl
26	flash_ctl_ad_12	70	mpu401_wrn	114	sdram_data_15	158	spi_scs
27	flash_ctl_ad_11	71		115	sdram_data_14	159	spi_sclk
28	flash_ctl_ad_0	72	mpu401_addr_3	116	sdram_data_13	160	spi_sdo
29	flash_ctl_ad_9	73	mpu401_addr_2	117	sdram_data_12	161	
30		74	mpu401_addr_1	118	sdram_data_11	162	I2s_out3
31	flash_ctl_ad_8	75	mpu401_addr_0	119	sdram_data_10	163	I2s_out2
32	flash_ctl_ad_7	76		120		164	I2s_out1
33	flash_ctl_ad_6	77	mpu401_data_7	121	sdram_data_9	165	I2s_out0
34	flash_ctl_ad_5	78	mpu401_data_6	122	sdram_data_8	166	

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
35	flash_ctl_ad_4	79	mpu401_data_5	123	sdram_data_7	167	I2s_mclk
36		80	mpu401_data_4	124	sdram_data_6	168	
37	flash_ctl_ad_3	81		125	sdram_data_5	169	I2s_bclk
38	flash_ctl_ad_2	82	mpu401_data_3	126		170	I2s_lrclk
39	flash_ctl_ad_1	83	mpu401_data_2	127	sdram_data_4	171	i2s_in
40	flash_ctl_ad_0	84	mpu401_data_1	128	sdram_data_3	172	
41		85	mpu401_data_0	129	sdram_data_2	173	spdifout_3
42	flash_rdy	86		130	sdram_data_1	174	spdifout_2
43	flash_we	87		131	sdram_data_0	175	spdifout_1
44		88	reset	132		176	spdifout_0