## DESCRIPTION

With high speed PCI V2.1 bus controller and legacy audio SBPro® DSPemulator,CMI8738 is designed for PC add-in cards and all-in-one motherboards. No external CODEC is needed in CMI8738: CMI-8738 supports the legacy audio – SBPRO™, FM emulator/DLS wavetable music synthesis, and HRTF 3D positional audio functions. Drivers support EAX®, Karaoke Key, Echo……functions.

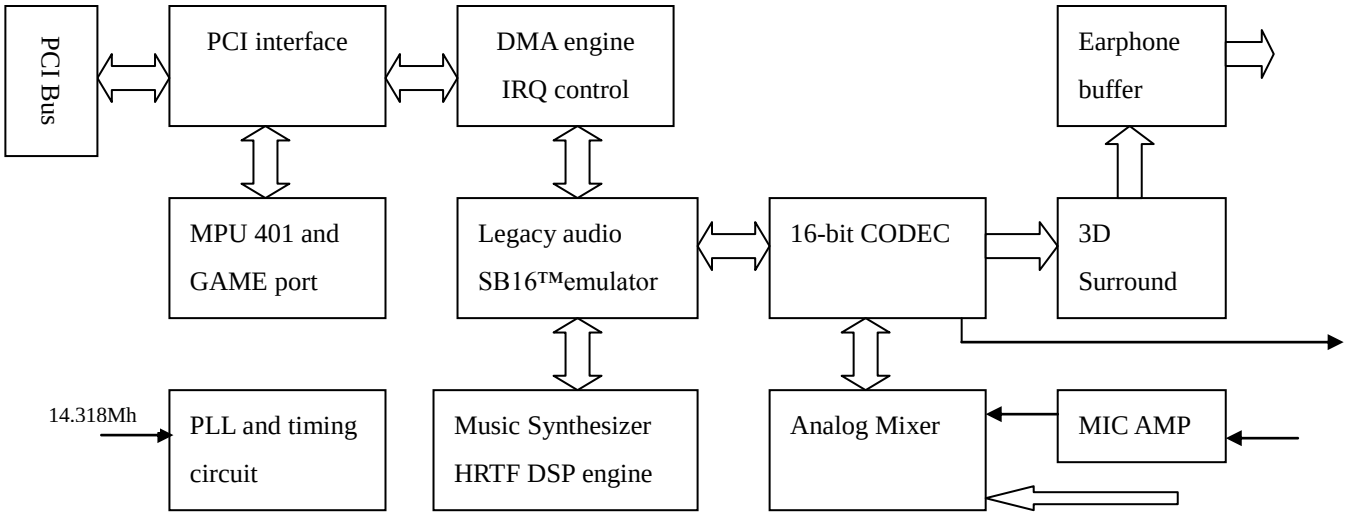
CMI8738 uses HRTF 3D extension technology to enhance traditional HRTF 3D positional audio by substituting two-speaker system by four or six - speaker one.

Being outstanding for its full audio functions, competitive price, and power management, CMI-8738 is the best choice for people seeking for optimum use of the PC applications.

## FEATURES

- HRTF-based 3D positional audio, supporting DirectSound™ 3D interface
- Supports 4 speakers, C3DX positional audio in 4 speaker mode
- Legacy audio SBPRO™ compatible
- DLS-based wavetable music synthesizer, supports DirectMusic™
- Built-in 32ohm Earphone buffer
- Drivers support EAX®, Karaoke Key, Echo…
- MPU-401 port/ Dual game port
- 16-bit full duplex CODEC
- 32-bit PCI bus master
- External E²PROM interface
- Single chip design, digital power +3.3V, analog power +5V, 128 pins QFP

## BLOCK DIAGRAM



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## Revision History

| Date | Rev. | Release Note |
|---|---|---|
| 2010/05/03 | Rev. 1.5 | Format Modification |

## 1. Description and Overview

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Being compatible with DirectSound™ 3D, CMI8738 meets PC99® requirements, and supports professional digital audio interface such as 16-bit SPDIF IN (0.5V ~ 5V)and OUT(44.1K and 48K format).

CMI8738 uses HRTF 3D extension technology to enhance traditional HRTF 3D positional audio by substituting two-speaker system by four or six - speaker (it supports additional 2 ch 16-bit DAC to provide rear side audio). It greatly improves HRTF 3D positional audio quality and successfully removes the sweet spot limitations: users can enjoy genuine 3D audio gaming effects, and don't have to worry about the environmental confinement any more.

Being outstanding for its full audio functions, competitive price, and power management, CMI-8738 is the best choice for people seeking for optimum use of the PC applications.

## 2. Features

- 4CH DAC
- HRTF-based 3D positional audio, supporting DirectSound™ 3D interface
- Supports 4 speakers, C3DX positional audio in 4 CH speaker mode
- Legacy audio SBPRO™ compatible
- DLS-based wavetable music synthesizer, supports DirectMusic™
- Built-in 32ohm Earphone buffer
- Drivers support EAX®, Karaoke Key, Echo…
- MPU-401 port/ Dual game port
- 16-bit full duplex CODEC
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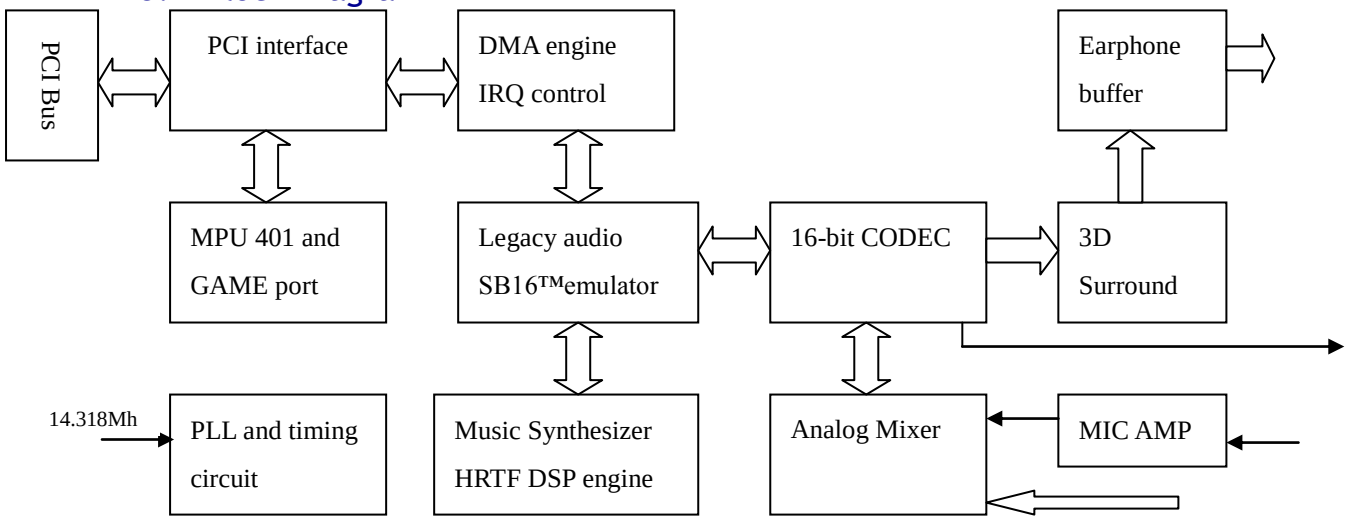
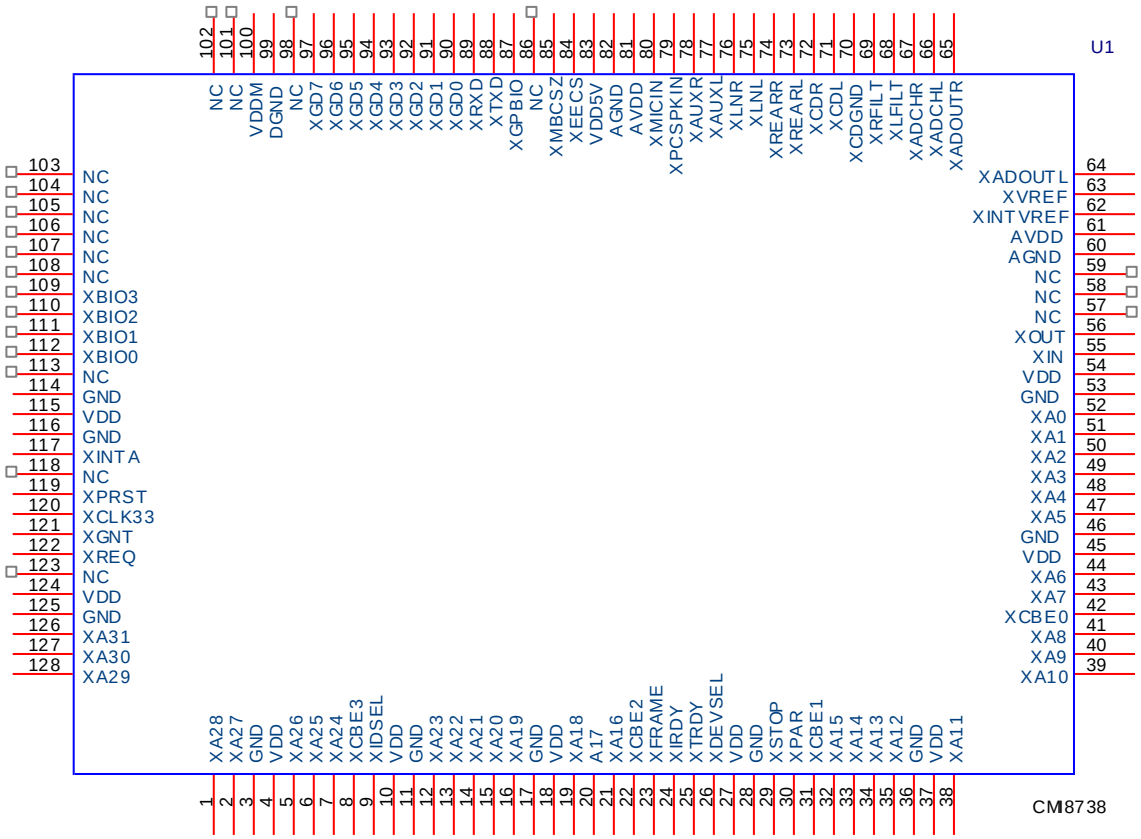
## 3. Block Diagram




## 4. Pin Assignment

**QFP 128 PINS**




**CMI8738SX 4CH AUDIO CHIP**

# 5. Pin Description

## 5.1 Digital Pin Description

| Name | Number | PIN Type | Definition |
|---|---|---|---|
| XA31-XA0 | 126-128,1-2,5-7,12-16,19-21,32-35,38-41,43-44,47-52 | I/O | PCI bus address and data lines |
| XINTA | 117 | O | Interrupt request , active-low. |
| XPRST | 119 | I | Reset |
| XCLK33 | 120 | I | PCI bus clock. |
| XGNT | 121 | I | Bus master grant, active-low. |
| XREQ | 122 | O | Bus master request, tri-state output, active-low. |
| XIDSEL | 9 | I | ID select, active-high. |
| XFRAME | 23 | I/O | Cycle frame, active-low. |
| XIRDY | 24 | I/O | Initiator ready, active-low. The bus master device is ready to transmit or receive data |
| XTRDY | 25 | I/O | Target ready, active-low. The target device is ready to transmit or receive data |
| XDEVSEL | 26 | I/O | Device select, active-low. The target device has decoded the address of the current transaction as its own chip select range. |
| XSTOP | 29 | I/O | Stop transaction, active-low. The target device request to the master to stop the current transaction. |
| XPAR | 30 | I/O | Parity. The pin indicates even parity across XA31-XA9 and XCBE3-0 for both address and data phases. |
| | | | |
| XCBE3,2,1,0 | 8,22,31,42 | I/O | Multiplexed command/byte enable. These pins indicate cycle type during the address phase of a transaction. |
| VDD | 4,10,18,27,37,45,54,115,124 | +5V | Digital and PCI I/O power pin |
| GND | 3,11,17,28,36,46,53,114,116,125 | GND | Digital and PCI I/O ground |
| XIN | 55 | I | 14.318Mhz crystal, or external clock input |
| XOUT | 56 | O | 14.318Mhz crystal |
| XGD7-XGD4 | 97-94 | I | Game port switch input pin.<br>Switch D to switch A |
| XGD3-XGD0 | 93-90 | I/O | Game port resistor input pin.<br>RC3 to RC0 |
| XTXD | 88 | O | MIDI transmit data |
| XRXD | 89 | I | MIDI receive data |
| XBIO3-XBIO0 | 109-112 | I/O | General purpose I/O |
| **Name** | **Number** | **PIN Type** | **Definition** |
| VDD5V | 83 | +5V | Digital and PCI I/O power pin |
| VDDM | 100 | +5V | Digital and PCI I/O power pin |
| DGND | 99 | GND | Digital and PCI I/O ground |
| XEECS | 84 | O | EEPROM chip select |
| XA31-XA0 | 126-128,1-2,5-7,12-16,19-21,32-35,38-41,43-44,47-52 | I/O | PCI bus address and data lines |
| XINTA | 117 | O | Interrupt request , active-low. |
| XPRST | 119 | I | Reset |
| XCLK33 | 120 | I | PCI bus clock. |

| | | | |
|---|---|---|---|
| **XGNT** | 121 | I | Bus master grant, active-low. |
| **XREQ** | 122 | O | Bus master request, tri-state output, active-low. |
| **XIDSEL** | 9 | I | ID select, active-high. |
| **XFRAME** | 23 | I/O | Cycle frame, active-low. |
| **XIRDY** | 24 | I/O | Initiator ready, active-low. The bus master device is ready to transmit or receive data |
| **XTRDY** | 25 | I/O | Target ready, active-low. The target device is ready to transmit or receive data |
| **XDEVSEL** | 26 | I/O | Device select, active-low. The target device has decoded the address of the current transaction as its own chip select range. |
| **XSTOP** | 29 | I/O | Stop transaction, active-low. The target device request to the master to stop the current transaction. |
| **XPAR** | 30 | I/O | Parity. The pin indicates even parity across XA31-XA9 and XCBE3-0 for both address and data phases. |
| **XCBE3,2,1,0** | 8,22,31,42 | I/O | Multiplexed command/byte enable. These pins indicate cycle type during the address phase of a transaction. |
| **VDD** | 4,10,18,27,37,45,54,115,124 | +5V | Digital and PCI I/O power pin |
| **GND** | 3,11,17,28,36,46,53,114,116,125 | GND | Digital and PCI I/O ground |
| **XIN** | 55 | I | 14.318Mhz crystal, or external clock input |
| **XOUT** | 56 | O | 14.318Mhz crystal |
| **XGD7-XGD4** | 97-94 | I | Game port switch input pin.<br>Switch D to switch A |
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| **XRXD** | 89 | I | MIDI receive data |
| **XBIO3-XBIO0** | 109-112 | I/O | General purpose I/O |

**Remark: All PCI interface I/O pins are 3.3V signal and 5V tolerance.**

## 5.2 Analog Pin Description

| Name | Number | PIN Type | Definition |
|---|---|---|---|
| **AVDD** | 61,81 | +5V | Analog power |
| **AGND** | 60,82 | GND | Analog ground |
| **XADOUTL-R** | 64,65 | AO1 | Line out |
| **XADCHL-R** | 66,67 | AI/O | ADC filter |
| **XLFILT** | 68 | AI/O | Left channel DAC filter |
| **XRFILT** | 69 | AI/O | Right channel DAC filter |
| **XVREF** | 63 | AI | Reference Voltage (no use, left it floating) |
| **XINTVREF** | 62 | AI | Reference Voltage |
| **XCDL-R XCDGND** | 71,72,70 | AI | CD audio differential input |
| **XLNL-R** | 75,76 | AI | Line in or Rear speaker out |
| **XAUXL-R** | 77,78 | AI | Aux. Line in |

| | | | |
|---|---|---|---|
| **XPCSPKIN** | 79 | AI | PC beep signal |
| **XMICIN** | 80 | AI | Microphone in |
| **XREARL-R** | 73,74 | AI/O | Rear speaker out |
| **XGPBIO** | 87 | O | General purpose I/O pin |
| **XMBCSZ** | 85 | I | Audio chip select (low:enable) |
| **NC** | 57-59,86,98,101-108,113,118, 123 | - | Reserved |

# 6. Electrical Characteristics

## 6.1 Absolute Maximum Ratings

| Ratings | Symbol | Value | Units |
|---|---|---|---|
| **Digital power voltage** | VDD | VDD±5% | V |
| **Analog power voltage** | AVDD | AVDD±5% | V |
| **Operating temperature range** | TO | 0 to 70 | °C |
| **Storage temperature range** | TST | -40 to 125 | °C |
| **Maximum power dissipation** | PDMAX | 300 | MW |

## 6.2 Digital Characteristics

| PARAMETER | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Input high voltage(PCI I/O)** | VIH | 2. | | VDD+0.5 | V |
| **Input low voltage (PCI I/O)** | VIL | -0.5 | | 0.8 | V |
| **Output high voltage** | VOH | 2.4 | | VDD | V |
| **Output low voltage** | VOL | 0.0 | 0.2 | 0.4 | V |
| **Output buffer current** | | | 5 | | mA |

## 6.3 Audio Characteristics

| PARAMETER | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Analog input voltage** | Avin | | 1.1 | | VRms |
| **Analog output voltage** | Avout | | 1.1 | | VRms |
| **A-A S/N ratio** | | | 85 | | db |
| **A-A THD** | | | 0.09 | | |
| **ADC S/N ratio** | | | 80 | | db |
| **ADC THD** | | | 0.1 | 0.2 | % |
| **DAC S/N ratio** | | | 80 | | db |
| **DAC THD** | | | 0.1 | 0.2 | % |
| **Microphone input level** | | 20 | | 200 | mv |

| | | | | | |
|---|---|---|---|---|---|
| **Microphone booster** | | | | 20 | db |
| **Analog input voltage** | Avin | | 1.1 | | VRms |
| **Analog output voltage** | Avout | | 1.1 | | VRms |

## 7. PCI Configuration Spaces (Audio)

00h 13F6 : (Vender ID) read only

02h 0111 : (Device ID) read only

04h 0006 : Command (State after #RST all is “0”)

0 (bit 9) Fast back-to-back enable

0 (bit 8) #SERR enable (R/W)

0 (bit 7) Wait cycle control

0 (bit 6) Parity error response

0 (bit 5) VGA palette snoop

0 (bit 4) Memory write and invalidate enable

0 (bit 3) Special cycles

1 (bit 2) Bus master (R/W)

0 (bit 1) Memory space

1 (bit 0) I/O space (R/W)

06h 0280 : Status

0 (bit 15) Detected Parity Error

0 (bit 14) Signaled System Error

0 (bit 13) Received Master Abort

0 (bit 12) Received Target Abort

0 (bit 11) Signaled Target Abort

01 (bits 10-9) DEVSEL timing 00-fast, 01-medium, 10-slow

0 (bit 8) Data Parity Error Detected

1 (bit 7) Fast Back-to-Back Capable

0 (bit 6) UDF Supported

0 (bit 5) 0-33MHz ,1-66MHZ Capable

00000 (bits 4-0) Reserved

08h 10 : Revision ID

09h 040100 : Audio device

0Ch 00 : Cache Line Size

0Dh 20 : Latency Timer

0Eh 80 : Header Type

0Fh 00 : BIST

10h 0000d401 : I/O of length : -65280(ffff0100h) : First Base Address register
14h 00000000 : Uninitialized : Second Base Address register
18h 00000000 : Uninitialized : Third Base Address register
1Ch 00000000 : Uninitialized : Fourth Base Address register
20h 00000000 : Uninitialized : Fifth Base Address register
24h 00000000 : Uninitialized : Sixth Base Address register
28h 00000000 : Cardbus CIS Pointer
2Ch 13f6 : (SubSystem Vender ID) (R/W)
2Eh ffff : SubSystem ID (R/W)
30h 00000000 : Expansion ROM Base Address
34h 00000000 : Reserved
38h 00000000 : Reserved
3Ch 05 : Interrupt Line
3Dh 01 : Interrupt Pin
3Eh 02 : Min Grant
3Fh 18 : Max Latency

**DMA Slave Configuration Register**(R/W) PCI Configuration address 40H

Bit(s)Function
31:16 Reserved
15:4 Slave Base Address 15-4. INTEL VX chipset seleted if Base Address 15:4=000h
3 Non legacy Extended Addressing
0 = disabled
1 = enabled
2:1 Transfer Size
00 = 8 bit transfer
01= 16 bit transfer
10= 32 bit transfer, non legacy
11= Reserved
0 Channel Enable
0 = disabled
1 = enabled

# 8. PCI register

## 8.1 Internal Register Mapping

### Function Control Register 0

Address **00**H

| Bit(s) | R/W | Name | Description |
|---|---|---|---|
| 31-20 | | Reserved. | |
| 19 | | RST_CH1 | Channel1, 1->Reset (Default 0) |
| 18 | | RST_CH0 | Channel0, 1->Reset (Default 0) |
| 17 | | CHEN1 | Channel1, 1->Enabled, 0->Disabled. |
| 16 | | CHEN0 | Channel0, 1->Enabled, 0->Disabled. |
| 15-4 | | Reserved | |
| 3 | | PAUSE1 | Channel1, 1->Pause if channel1 is enabled. |
| 2 | | PAUSE0 | Channel0, 1->Pause if channel0 is enabled. |
| 1 | | CHADC1 | Channel 1 , 1->Recording, 0->Playback |
| 0 | | CHADC0 | Channel 0, 1->Recording, 0->Playback |

### Function Control Register 1

Address **04**H

| Bit(s) | R/W | Name | Description |
|---|---|---|---|
| 31-16 | | Reserved | |
| 15-13 | | DSFC[2:0] | **DAC** Sampling Frequency Select, |
| | | | 0 0 0 5.512 K |
| | | | 0 0 1 11.025 K |
| | | | 0 1 0 22.05 K |
| | | | 0 1 1 44.1 K |
| | | | 1 0 0 8 K |
| | | | 1 0 1 16 K |

| | | | | | |
|---|---|---|---|---|---|
| | | 1 | 1 | 0 | 32 K |
| | | 1 | 1 | 1 | 48 K |
| 12-10 | ASFC[2:0] | **ADC** Sampling Frequency Select, | | | |
| | | 0 | 0 | 0 | 5.512 K |
| | | 0 | 0 | 1 | 11.025 K |
| | | 0 | 1 | 0 | 22.05 K |
| | | 0 | 1 | 1 | 44.1 K |
| | | 1 | 0 | 0 | 8 K |
| | | 1 | 0 | 1 | 16 K |
| | | 1 | 1 | 0 | 32 K |
| | | 1 | 1 | 1 | 48 K |
| 9-6 | Reserved | | | | |
| 5 | INTRM | Interrupt Mask bit for MCB (Master control block) module interrupt. | | | |
| | | 0 | MCB interrupt disabled. | | |
| | | 1 | MCB interrupt enabled. | | |
| 4 | BREQ | If this bit is set low it will prevent the MCB and DAC/ADC block from accessing the memory. | | | |
| | | 0 | Bus Master request disabled(power on state) | | |
| | | 1 | Bus Master request enabled. | | |
| 3 | VOICE_EN | This bit enables Legacy Voice device(SB16,FM). | | | |
| | | 0 | Legacy Voice disabled on channel 0. | | |
| | | 1 | Legacy Voice enabled on channel 0. | | |
| 2 | UART_EN | This bit enables Legacy UART device. | | | |
| | | 0 | UART disabled | | |
| | | 1 | UART enabled | | |
| 1 | JYSTK_EN | This bit enables Legacy Joystick device. | | | |
| | | 0 | Joystick disabled | | |
| | | 1 | Joystick enabled | | |

| | |
|---|---|
| 0 | Reserved |

## Channel Format Register

Address **08**H

| Bit(s) | R/W | Name | Description |
|---|---|---|---|
| 31-24 | | VER[7:0] | PCI Audio subversion for internal indentification. “01” |
| 23-19 | | Reserved | |
| 18 | | FMOFFSET2 | When set 1 and Reg. 24H bit7 ‘FMmute=1’,FM PCM will be forced to DC value 0002H. |
| 17-16 | | Reserved | |
| 15-14 | | AdcBitLen[1:0] | Sample resolution<br>00 16 Bits per sample . (Default)<br>01 15 Bits per sample.<br>10 14 Bits per sample.<br>11 13 Bits per sample. |
| 13-12 | | AdcDacLen[1:0] | Sample resolution<br>00 600nSec per bit in a sample.<br>01 660nSec per bit in a sample.<br>10 1.3uSec per bit in a sample. (Default)<br>11 2.8uSec per bit in a sample. |
| 11 | | CH1 Ssmple Rate 176K | |
| 10 | | CH1 Sample Rate 88K | |
| 9 | | CH0 Sample Rate 176K | |
| 8 | | CH0 Sample Rate 88K | |
| 7-4 | | reserved | |
| 3-2 | | CH1FMT[1:0] | Data format of channel 1<br>00 8 bit Mono mode<br>01 8 bit Stereo mode<br>10 16 bit Mono mode<br>11 16 bit Stereo mode |

| | | |
|---|---|---|
| 1-0 | CH0FMT[1:0] | Data format of channel0 |
| | | 00 8 bit Mono mode |
| | | 01 8 bit Stereo mode |
| | | 10 16bit Mono mode |
| | | 11 16 bit Stereo mode |

## Interrupt Hold/Clear Register

Address **0C**H

| Bit(s) | R/W | Name | Description |
|---|---|---|---|
| 31-19 | | Reserved | |
| 18 | | TDMA_INT_EN | Interrupt hold/clear bits for updating TDMA position |
| | | | 0 Interruupt Clear |
| | | | 1 Interrupt Hold if exist. |
| 17 | | CH1_INT_EN | Interrupt hold/clear bits for the Channel 1. |
| | | | 0 Interrupt Clear |
| | | | 1 Interrupt Hold if exist. |
| 16 | | CH0_INT_EN | Interrupt hold/clear bits for the Channel 0. |
| | | | 0 Interrupt Clear |
| | | | 1 Interrupt Hold if exist. |
| 15-0 | | Reserved | |

## Interrupt Register

Address **10**H

| Bit(s) | R/W | Name | Description |
|---|---|---|---|
| 31 | R | INTR | Interrupt reflected from any sources. |
| | | | 0 No interrupt |
| | | | 1 Interrupt pending |
| 30-28 | | Reserved | |
| 27 | R | VCO | |
| 26 | R | MCBint | Abort conditions occur during PCI Bus Target/Master Access. |

| | | | |
|---|---|---|---|
| | | | 0 No interrupt |
| | | | 1 Interrupt pending |
| 25-17 | | Reserved | |
| 16 | R | UARTint | This bit is the UART interrupt bit. |
| | | | 0 No UART interrupt |
| | | | 1 UART interrupt pending |
| 15 | R | LTDMAINT | Interrupt for updating Low Channel TDMA position. |
| | | | 0 No interrupt |
| | | | 1 Interrupt pending |
| 14 | R | HTDMAINT | Interrupt for updation High Channel TDMA position. |
| | | | 0 No interrupt. |
| | | | 1 Interrupt pending. |
| 13-8 | | Reserved | |
| 7 | R | XDO46 | Direct programming EEPROM interface , read data register |
| 6 | R | LHBTOG | High/Low status from DMA CTRL register. |
| 5 | R | LegHDMA | Legacy is in High DMA channel. |
| 4 | R | LegStereo | Legacy is in Stereo mode. |
| 3 | R | Ch1Busy | Channel B Busy. |
| 2 | R | Ch0Busy | Channel A Busy. |
| 1 | R | Chint1 | Channel B Interrupt. |
| | | | 0 No interrupt |
| | | | 1 Interrupt pending |
| 0 | R | Chint0 | Channel A Interrupt. |
| | | | 0 No interrupt |
| | | | 1 Interrupt pending |

## Legacy Control/Status Register

Address **14**H

| Bit(s) | R/W | Name | Description |
|---|---|---|---|
| 31 | | Reserved | |
| 30-29 | | VMPU [1:0] | Base address for MPU401 access<br>00 Base address : 330h<br>01 Base address : 320h<br>10 Base address : 310h<br>11 Base address : 300h |
| 28 | | | Reserved |
| 27-26 | | VSBSEL[1:0] | The Base Address Select for SB16 access.<br>00 Base address: 220h<br>01 Base address: 240h<br>10 Base address: 260h<br>11 Base address: 280h |
| 25-24 | | FMSEL[1:0] | The Base Address Select for FM access.<br>00 Base address : 388h<br>01 Base address : 3C8h<br>10 Base address : 3E0h<br>11 Base address : 3E8h |
| 23-21 | | Reserved | |
| 20 | | SetRetry | Mode of wait state .<br>0:legacy I/O wait (default)<br>1:legacy I/O BUS retry |
| 19 | | C_EEACCESS | Direct programming EEPROM interface Registers. |
| 18 | | C_EECS | |
| 17 | | C_EEDI46 | |
| **16** | | C_EECK46 | |
| 15-0 | | Reserved | |

## Micellaneous Control Register

**Address 18H**

| Bit(s) | R/W | Name | Description |
|---|---|---|---|
| 31 | | PWD | Power Down Mode enabled.. |
| 30 | | RESET | Reset Bus Master/DSP Engine. |
| 29-28 | | SFIL[1:0] | Four level of filter control at the front end DAC.. |
| 27 | | TX/VX | Which motherboard to work with<br>0 VX chip sets.<br>1 TX chip sets. |
| 26 | | N4SPK3D | Hardware copy front channel to rear channel |
| 25-24 | | Reserved | |
| 23 | | ENDBDAC | Default low, High will enable Double DAC structure. |
| 22 | | XCHGDAC | Default low,<br>0 CH0 > Front SPKR, CH1 > Back SPKR.<br>1 CH0 > Back SPKR, CH1 > Front SPKR. |
| 21-20 | | Reserved | |
| 19 | | FM_EN | Legacy FM enabled. |
| 18-17 | | Reserved | |
| 16 | | VIDWPDSB | Sub ID write protect disabled. (default 0) |
| 15 | | Reserved | |
| 14 | | MASK_EN | Activate channel mask on Legacy DMA.<br>0 Disabled<br>1 Enabled |
| 13 | | VIDWPDSB | Write Protect of HSP Configuration Sub ID.<br>0 Protect.<br>1 No protect. |
| 12 | | SFILENB | Let software contrl filter stepping at the front end DAC. |
| 11-5 | | Reserved | |
| 4 | | MIDSMP | Enable 1/2 interpolation at the Front end DAC.. |
| 3-2 | | UPDDMA[1:0] | For every the number of samples to notify updating TDMA position.<br>00 Every 2048 samples |

| | | | |
|---|---|---|---|
| | | | 01 Every 1024 samples |
| | | | 10 Every 512 samples. |
| | | | 11 Every 256 samples. |
| 1-0 | | TWAIT[1:0] | For controling the length of legacy BUS cycle. |
| | | | 00 3 PCICLK. |
| | | | 01 18 PCICLK. |
| | | | 10 24 PCICLK |
| | | | 11 32 PCICLK |
| * Notice | | REQ_SQ[2:0] | States of BusRequest Engine. |
| MM_DATA | | | Bus Master is using Bus. |
| MIDLE | | | Bus Master is not using Bus. |
| REQA/REQB | | | Channel 0/1 BusMaster Request. |
| GNTA/GNTB | | | Channel 0/1 BusMaster Grant. |
| ADRQ/BDRQ | | | Channel 0/1 DMA Request. |
| ADACK/BDACK | | | Channel 0/1 DMA Acknoledge. |
| AIRQ/BIRQ | | | Channel 0/1 Interrupt. |
| CX/BX | | | Channel 0/1 Busy. |

### T - DMA Position

Address **1C**H

| Bit(s) | R/W | Name | Description |
|---|---|---|---|
| 31-16 | R | TDMACN T | Current Byte/Word Count of DMA channel. |
| 15-0 | R | TDMAADR | Current Address of DMA channel. |

### Mixer Control / Device Configure Register (can be accessed only by **BYTE** instruction)

Address **20**H

| Bit(s) | R/W | Name | Description |
|---|---|---|---|
| 7-0 | W | SBVR[7:0] | Programmable SB16 version No. |
| | R | DEV[7:0] | Hardwire device version No. |

Address **21**H

| Bit(s) | R/W | Name | Description |
|---|---|---|---|
| 7-3 | | Reserved | |
| 2 | | X_ADPCM | SB16 ADPCM enable,default disabled. |
| 1 | | PROINV | SBPro Left/Right channel switching. |
| 0 | | X_SB16 | Indicate device active as SB16 compatible, default SB16 |

Address **22**H

| Bit(s) | R/W | Name | Description |
|---|---|---|---|
| 7-0 | | IDXdata | Mapping SB compatible mixer INDEX register data port(A2x5h) |

Address **23**H

| Bit(s) | R/W | Name | Description |
|---|---|---|---|
| 7-0 | | IDXaddr | Mapping SB compatible mixer INDEX register address port(A2x4h) |

Address **24**H

| Bit(s) | R/W | Name | Description |
|---|---|---|---|
| 7 | | Fmmute | Mute FM |
| 6 | | Wsmute | Mute Wave stream |
| 5 | | SPK4 | select four speaker mode(emulate Line in to Line out ) |
| 4 | | Rear2front | exchange rear and front channels's speaker out |
| 3 | | Waveinl | Digital Wave recording Left channel |
| 2 | | Waveinr | Digital Wave recording Right channel |
| 1-0 | | Reserved | |

Address **25**H

| Bit(s) | R/W | Name | Description |
|---|---|---|---|
| 7 | | RAUXREN | Recording source select R-Aux |
| 6 | | RAUXLEN | Recording source select L_Aux |
| 5 | | VAUXRM | R-AUX mute control |

| | | |
|---|---|---|
| 4 | VAUXLM | L-AUX mute control |
| 3-1 | VADMIC[2:0] | Recording MIC volume control |
| 0 | MICGAINZ | MIC gain control,default high disable |

Address **26**H

| Bit(s) | R/W | Name | Description |
|---|---|---|---|
| 7-4 | | VAUXL[3:0] | L-AUX volume control |
| 3-0 | | VAUXR[3:0] | R-AUX volume control |

Address **27**H

| Bit(s) | R/W | Name | Description |
|---|---|---|---|
| 0 | | DMAUTO | SB16 Low/High DMA Auto detect enabled ,When high. |
| 1 | | Reserved | |
| 2 | | XGPBIO | general purpose bi-direction pin, when high output tri-state (default LOW) |
| 3 | | Reserved | |
| 4 | | Reserved | |
| 5 | | XGPO1 | general purpose output pin 1,this pin shared with XSPDIFO pin, and enabled when index reg. F0_bit 0 programmed high. |
| 6-7 | | Reserved | |

### Mup401 PCI Port

Index address **40-4F**H

### FM PCI Port

Index address **50-5FH**

### Extension Index Register (access from SB compatible mixer port)

Index address **F0**H

| Bit(s) | R/W | Name | Description |
|---|---|---|---|
| 7-5 | | VPHONE[2:0] | Phone volume control |
| 4 | | VPHOM | Phone mute control |
| 3 | | VSPKM | PC-Speaker mute control,default high unmute |
| 2 | | RLOOPREN | Recording R-channel enable |
| 1 | | RLOOPLEN | Recording L-channel enable |
| 0 | | VADMIC3 | Micphone record boost, default low disable, high enable. |

Index address **F8-FF**H

These 8 registers is used to programming M/N conunter by clock generator

### Channel 0 Frame Register 1

Address **80**H

| Bit(s) | R/W | Name | Description |
|---|---|---|---|
| 31-0 | W | BASADDR0 | Base address of channel 0. |
| | R | CURADDR0 | Current address of channel 0. |

### Channel 0 Frame Register 2

Address **84**H

| Bit(s) | R/W | Name | Description |
|---|---|---|---|
| 31-16 | W | BASCNT0 | Base count of samples at Codec. |
| 15-0 | W | BASCNT0 | Base count of samples at Bus Master. |
| 31-16 | R | CURCNT0 | Current count of samples at Codec. |
| 15-0 | R | CURCNT0 | Current count of samples at Bus Master. |

### Channel 1 Frame Register 1

Address **88**H

| Bit(s) | R/W | Name | Description |
|---|---|---|---|
| 31-0 | W | BASADDR1 | Base address of channel 0. |
| | R | CURADDR1 | Current address of channel 0. |

### Channel 1 Frame Register 2

Address **8C**H

| Bit(s) | R/W | Name | Description |
|---|---|---|---|
| 31-16 | W | BASCNT1 | Base count of samples at Codec. |

| | | | |
|---|---|---|---|
| 15-0 | W | BASCNT1 | Base count of samples at Bus Master. |
| 31-16 | R | CURCNT1 | Current count of samples at Codec. |
| 15-0 | R | CURCNT1 | Current count of samples at Bus Master. |

**Legacy SB compatible mixer**

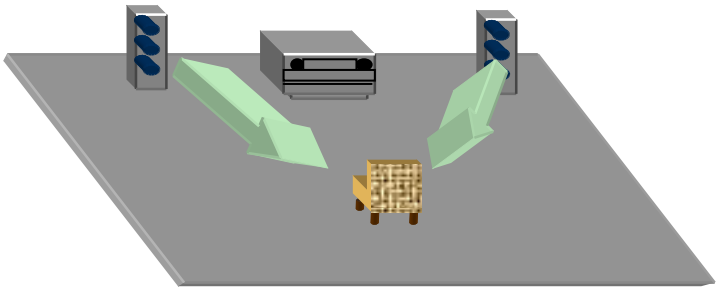
| Index | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 0x00 | Reserved | | | | | | | |
| 0x04 | Wave volume left channel | | | | Wave volume right channel | | | |
| 0x0A | | | | | | Mic volume | | |
| 0x22 | Master volume left channel | | | | Master volume right channel | | | |
| 0x26 | FM volume left channel | | | | FM volume right channel | | | |
| 0x28 | Analog-CD volume left channel | | | | Analog-CD volume right channel | | | |
| 0x2E | Line-In volume left channel | | | | Line-In volume right channel | | | |
| 0x30 | Reserved | | | | | | | |
| 0x31 | Reserved | | | | | | | |
| 0x32 | Reserved | | | | | | | |
| 0x33 | Reserved | | | | | | | |
| 0x34 | Reserved | | | | | | | |
| 0x35 | Reserved | | | | | | | |
| 0x36 | Reserved | | | | | | | |
| 0x37 | Reserved | | | | | | | |
| 0x38 | Reserved | | | | | | | |
| 0x39 | Reserved | | | | | | | |
| 0x3A | Reserved | | | | | | | |
| 0x3B | PC spk volume | | | | | | | |
| 0x3C | | | | Output muting controls | | | | |
| | | | | Line L | Line R | CD L | CD R | Mic |
| 0x3D | | Recording left channel controls | | | | | | |
| | | FM L | FM R | Line L | Line R | CD L | CD R | Mic |
| 0x3E | | Recording right channel controls | | | | | | |
| | | FM L | FM R | Line L | Line R | CD L | CD R | Mic |
| 0x3F | Reserved | | | | | | | |
| 0x40 | Reserved | | | | | | | |
| 0x41 | Reserved | | | | | | | |
| 0x42 | Reserved | | | | | | | |
| 0x43 | Reserved | | | | | | | |
| 0x44 | Reserved | | | | | | | |
| 0x45 | Reserved | | | | | | | |
| 0x46 | Reserved | | | | | | | |
| 0x47 | Reserved | | | | | | | |

**Please do not write any values into reserved registers**
**0x30-0x3A registers are SB16 compatible and will be linked with 0x04-0x21 SB Pro registers correspondingly.**
**Only 0x30-31 master volume registers are 5 bits and the other are 4 bits.**

# 9. Audio Processing Technology

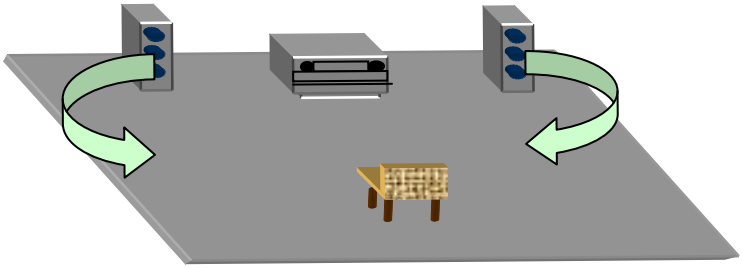
## 9.1 Stereo

**It is only one-dimensional, as sounds come from (left /right) the physical location of speakers.**



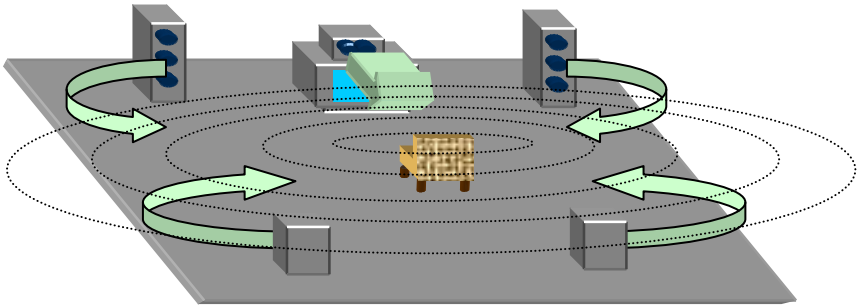
## 9.2 Surround (Stereo Expander)

**It filters the existing stereo signal to make the sounds fill in the area around the speakers, and in front of the listener. Sound sources appear to come from outside the physical locations of the speakers.**



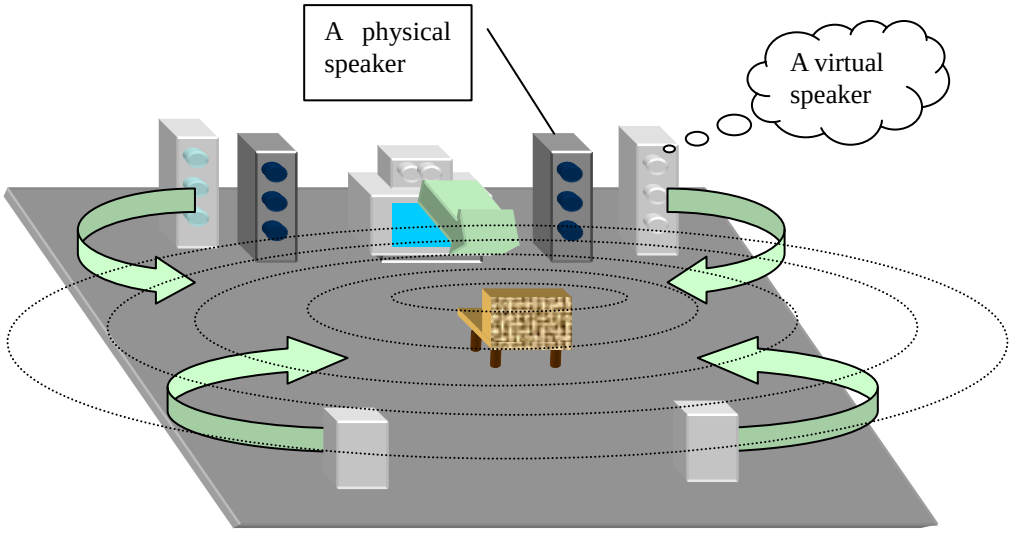
## 9.3 Multi-Speaker Surround (Dolby Pro Logic or Digital AC-3)

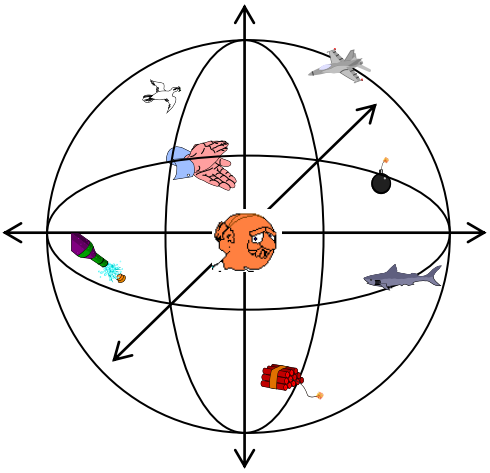
**It uses five speakers instead of two to surround the listener; hence, sound sources come from five directions and create engaging audio experience. This surround sound effect, however, has to be pre-recorded, and it dose not support interactive environment.**



## 9.4 HRTF 3D Positional 3D (C-Media 3D)

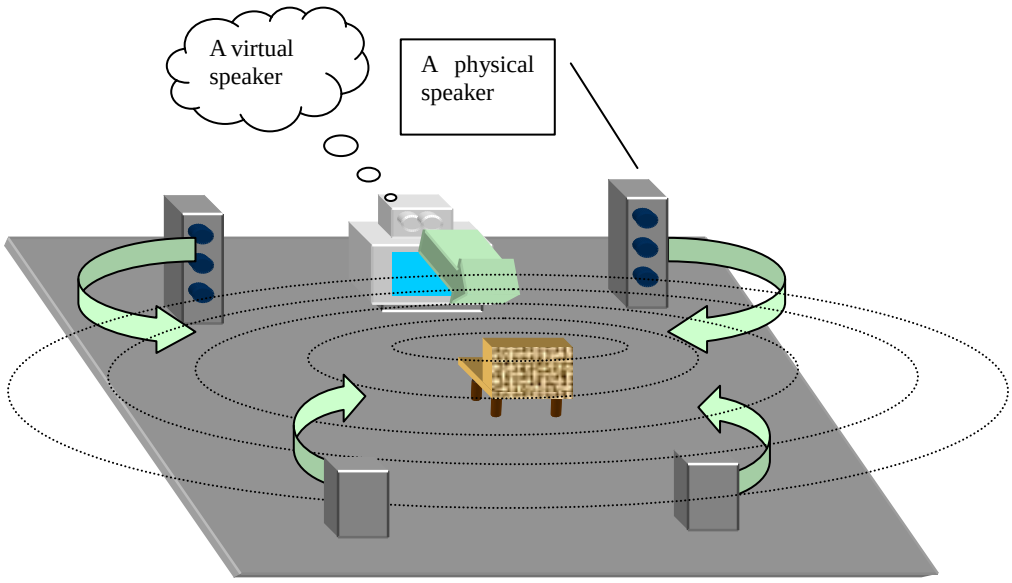
Only this sound processing technology can be called real 3D manifestation, as 3D usually refers to the three dimensions of X, Y and Z. This technology allows people to pin-point the location of sound in the real world (up/down, left/right, front/back)using only two speakers or a pair of headphones. This technology also supports interactive 3D applications to get a real-time placement of sounds via API (application programming interface) such as Microsoft DirectSound3DTM. We can also use this technology to simulate Multi-speaker Surround with two physical speakers to deliver five “virtual" speakers in the air, surrounding the listener and creating home theater sound environment. This is the most economical and the easiest solution to people who would like to get high performance surround sound but don’t want to spend money in adding extra speakers.



9.5 HRTF 3D Extension Positional (C-Media 3DX)

3D illusion exists because traditional 3D positional audio system assumes the user's position as the sweet spot to design crosstalk-cancellation circuit; therefore, if the user wants to have 3D positional audio effects, he can't move his head or position out of sweet spot. Another 3D illusion fails because half the population are compulsive "head-turners" who will never get 3D audio from two speakers . To remedy this, C-Media utilizes HRTF 3D extension technology (C3DX) to enhance traditional HRTF 3D positional audio by substituting two-speaker system by four-speaker one. Therefore, at least one or two speakers should be placed behind the listener's head to complement the rear-side effect, thus creating compelling realistic sound. This technology greatly improves HRTF 3D positional audio quality, and successfully eliminates the sweet spot limitation. Users can enjoy the real 3D audio gaming effects, and don't have to worry about the environmental confinement any more.




9.6 C3D Positional Audio Technology White-Paper

# C3D Positional Audio Technology White-Paper

# C3D HRTF Positional Audio Technology

The basic concept of C3D is: since we can hear sound three dimensionally in the real world using our two ears, it must be possible to regenerate the same sound effect from two loud speakers.

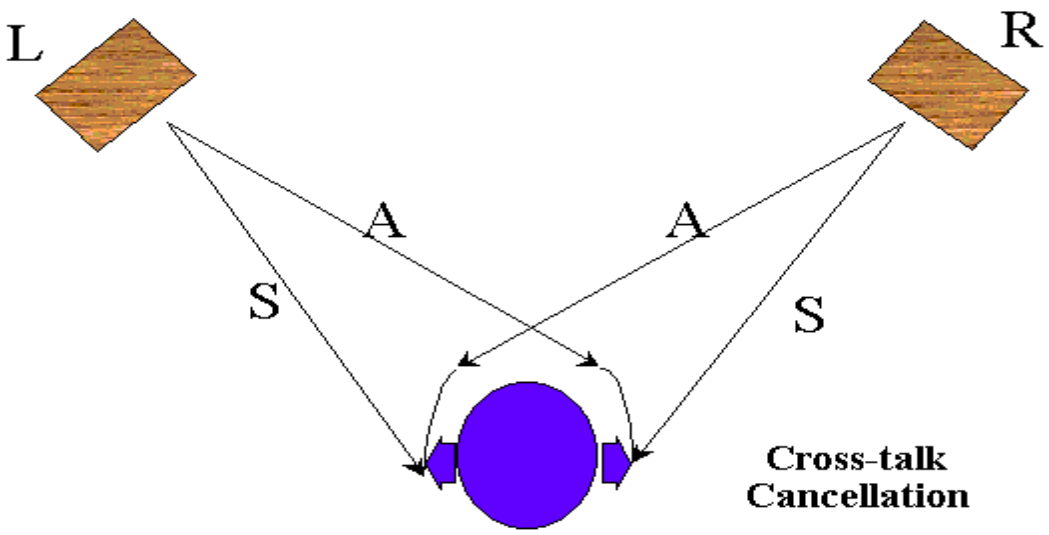
## How to listen to C3D sound correctly and properly?

### a. Use Headphones to Have Much Better Effect

When you use headphones in listening, there will be less interference such as outside voices or room reflections comparing to using speakers.

### b. Choose Correct Output Devices

Choose the correct output devices in the options of demo program in accordance with what listening devices you want to listen to. Listening through speakers must be proceeded by crosstalk-cancellation, so if you choose the wrong output devices, there won't be any 3D positional audio effect.

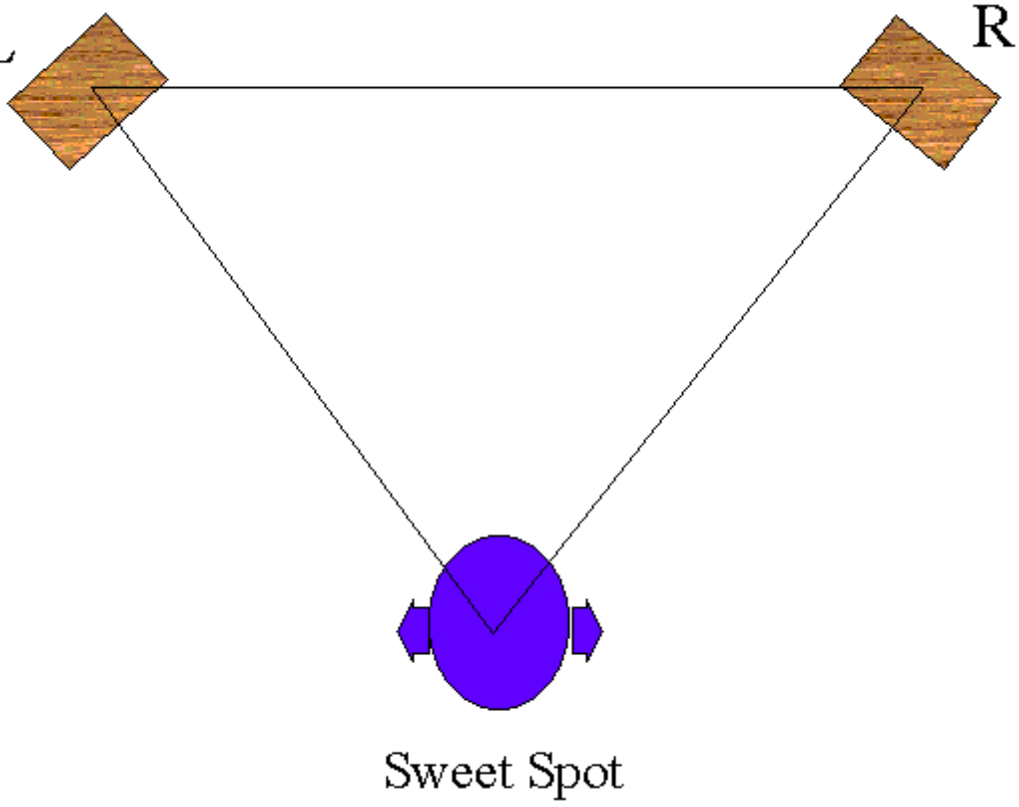



## c. Position of Speakers

If you listen from speakers, please do not reverse the left and right speakers, which should be put in equal distance from the listener. That is, the listener, the left, and the right speaker must be in the topmost of a right triangle. The position of the listener is called the “sweet spot”. In addition, the height of the listener’s ears must be equal to that of the speakers.

### 9.7 Turn Surround Sound Functions off

When the surround sound effect is enabled, it will cause confusion with C3D sound, and make positional sound effect invalid.




## 10. CMI8738 PCI Audio Adapter Layout Notes

1. The wires of analog circuits(chip pin64-80) must be wider than 12mil.
2. Placing digital signals such as SPDIF IN/OUT(pin86, 98) and TXD/RXD(pin88,89) near the analog signals should be avoided. However, if these signals have to be adjacent, please place ground between these digital and analog signal wires to isolate noises.
3. The whole PCB grounding should be well-organized(The ground must be placed as much as possible. Also, the ground of both the component and the solder sides should be drilled as much as possible.).
4. The grounding under CMI8738 should be well-organized as mentioned above.
5. The regulator(78L05) must be placed near the chip as much as possible.
6. The chip and the circuits need independent power supply regulators to prevent insufficient currents.

## End of Specifications

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