ALC100/ALC100P
AC'97 Audio CODEC

Revision 1.1

May 25, 2000

1. Features :

- Single chip audio CODEC with high S/N ratio.
- 16-bit ADC and DAC resolution.
- Compliant with AC' 97 2.1 specification
- Supports AMR and CNR applications.
- 16-bit stereo full-duplex CODEC with fixed 48k sampling rate.
- 4 analog line-level stereo input with 5-bit volume control : LINE_IN,CD,VIDEO,AUX
- 2 analog line-level mono input : PC_BEEP,PHONE_IN.
- Mono output with 5-bit volume control.
- Stereo output with 5-bit volume control.
- 2 MIC inputs : Software selectable.
- Power management.
- 3D Stereo Enhancement
- True Line-Level output
- Multiple CODEC extension.
- External Amplifier power down capability.
- Dual power support : Digital :5V/3.3V Analog : 5V`
- Standard 48-Pin *LQFP* Package

2. Pin Description :

2.1 Digital I/O pins : 11 pins

Name	Type	Pin No	Description	Characteristic Definition
RESET#	I	11	AC'97 master H/W reset	CMOS input,V_t=0.35Vdd *
XTL-IN	I	2	Crystal input pad (24.576Mhz)	Crystal input pad
XTL-OUT	O	3	Crystal output pad	Crystal output pad
SYNC	I	10	Sample Sync (48Khz)	CMOS input,V_t=0.35Vdd
BIT-CLK	IO	6	Bit clock output (12.288Mhz)	CMOS input/output Vt=0.35Vdd (***Refer 6.2.5***)*
SDATA-OUT	I	5	Serial TDM AC97 output	CMOS input,V_t=0.35Vdd
SDATA-IN	O	8	Serial TDM AC97 input	CMOS output (***Refer 6.2.5***)
ID0#	I	45	ID strap 0	CMOS input Vt=0.35Vdd with 50KΩ pull high
ID1#	I	46	ID strap 1	CMOS input Vt=0.35Vdd with 50KΩ pull high
EAPD	O	47	External Amplifier power down control	8mA CMOS output
PWRI#	I	48	Internal register reset (For test)	CMOS input

2.2 Analog I/O Pins : 18 pins

Name	Type	Pin No	Description	Characteristic Definition
PC-BEEP	I	12	PC speaker input	Analog input (1Vrms)
PHONE	I	13	speakerphone input	Analog input (1Vrms)
AUX-L	I	14	AUX Left channel	Analog input (1Vrms)
AUX-R	I	15	AUX Right channel	Analog input (1Vrms)
VIDEO-L	I	16	Video audio Left channel	Analog input (1Vrms)
VIDEO-R	I	17	Video audio Right channel	Analog input (1Vrms)
CD-L	I	18	CD audio Left channel	Analog input (1Vrms)
CD-GND	I	19	CD audio analog GND	Analog input (1Vrms)
CD-R	I	20	CD audio Right channel	Analog input (1Vrms)
MIC1	I	21	First Mic input	Analog input (1Vrms)
MIC2	I	22	Second Mic input	Analog input (1Vrms)
LINE-L	I	23	Line input Left channel	Analog input (1Vrms)
LINE-R	I	24	Line input Right channel	Analog input (1Vrms)
LINE-OUTL	O	35	Line-Out Left channel	Analog output (1Vrms)
LINE-OUTR	O	36	Line-Out Right channel	Analog output (1Vrms)
LNLVL-L	O	39	True Line Level output-Left	Analog output (1Vrms)
LNLVL-R	O	41	True Line Level output-Right	Analog output (1Vrms)
MONO-OUT	O	37	SpeakerPhone output	Analog output (1Vrms)

2.3 Filter/References : 11 pins

Name	Type	Pin No	Description	Characteristic Definition
VREF	O	27	Reference voltage	Analog output (2.25~2.75V)

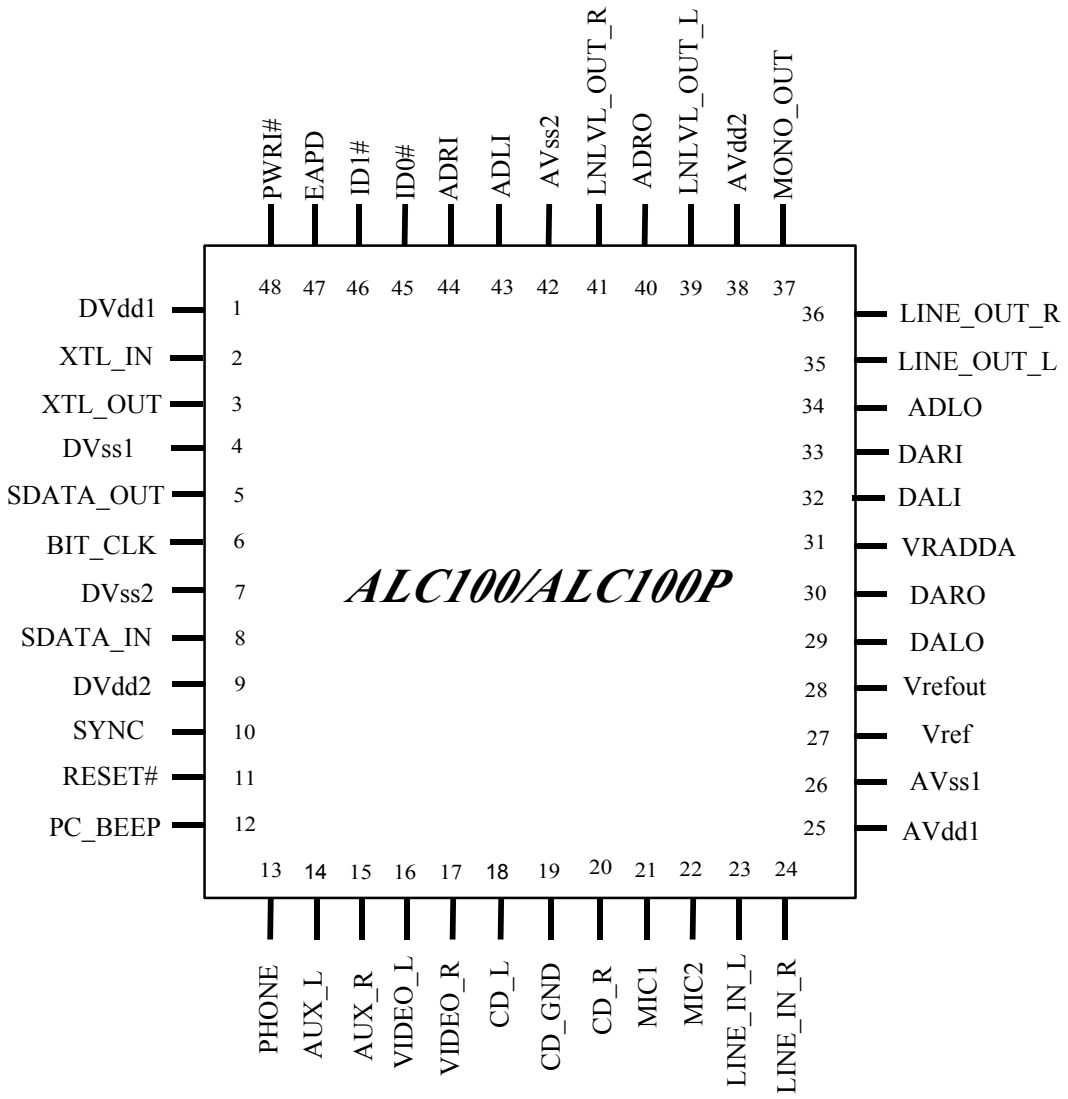
VREFOUT	O	28	Reference voltage out with 5mA drive	Analog output (2.25~2.75V)
DALO	O	29	DA Left output filter	Analog output
DARO	O	30	DA Right output filter	Analog output
VRADDA	O	31	VRADDA filter	Analog output
DALI	O	32	DALI filter	Analog output
DALO	O	33	DARI filter	Analog output
ADLO	O	34	AD Left filter	Analog output
ADRO	O	40	AD Right filter	Analog output
ADLI	O	43	ADLI filter	Analog output
ADRI	O	44	ADRI filter	Analog output

2.4 Power/Ground : 8 pins

Name	Type	Pin No	Description	Characteristic Definition
AVDD1	I	25	Analog VDD (5.0V)	
AVDD2	I	38	Analog VDD (5.0V)	
AVSS1	I	26	Analog GND	
AVSS2	I	42	Analog GND	
VDD1	I	1	Digital VDD (5.0V or 3.3V)	
VDD2	I	9	Digital VDD (5.0V or 3.3V)	
VSS1	I	4	Digital GND	
VSS2	I	7	Digital GND	

***When RESET# is active the BIT-CLK and SDATA-IN must be floating by internal pull low 100K resistors. So the ac-link signals are driven by another AC' 97 on CNR board. This requirement is not mentioned in AC' 97 specification rev2.1, please refer CNR (Communication Network Riser) specification rev1.0 page23~25 to get detail information.**

3. ALC100 Pin-Out Diagram :



Pinout Diagram of ALC100/ALC100P

4. Mixer Register :

All mixer register access with odd-number will return with 0.
Reading unimplemented registers will return 0.

MX00 Reset Default : 5800h

Bit	Type	Function
15		Reserved
14:10	R	return 16H
9	R	Read as 0 (No support 20-bit ADC)
8	R	Read as 0 (No support 18-bit ADC)
7	R	Read as 0 (No support 20-bit DAC)
6	R	Read as 0 (No support 18-bit DAC)
5	R	Read as 0 (No support for Loudness)
4	R	Read as 0 (No HeadPhone-Out support)
3	R	Read as 0 (No simulated stereo ,for analog 3D block use)
2	R	Read as 0 (No Bess & Treble Control)
1	R	Reserved,Read as 0
0	R	Read as 0 (No Dedicated Mic PCM input)

❶ Write to this register will reset all mixer registe2r to their default value. The write data is ignored.

MX02 Master Volume Default : 8000h

Bit	Type	Function
15	R/W	Mute Control 0 : Normal 1 : Mute (-∞ dB)
14:13		Reserved
12:8	R/W	Master Left Volume (MLV[4..0]) in 1.5 dB step
7:5		Reserved
4:0	R/W	Master Right Volume (MRV[4..0]) in 1.5 dB step

❶ For MRV/MLV,
00h 0 dB attenuation
1Fh 46.5 dB attenuation

❷ MRV/MLV are 5-bit R/W variables. The 6th bit implementation is optional. For this reason, when 6th bit is written by 1,it is equivalent to writing low 5-bit with 1. For example, writing 1xxxxx will read back 01111.

MX04 Line Level Output Volume Default : 8000h

Bit	Type	Function
15	R/W	Mute Control 0 : Normal 1 : Mute (-∞ dB)
14:13		Reserved
12:8	R/W	Line Level Output Left Volume (LNLV[4..0]) in 1.5 dB step
7:5		Reserved
4:0	R/W	Line Level Output Right Volume (LNRV[4..0]) in 1.5 dB step

❶ For LNRV/LNLV,
00h 0 dB attenuation
1Fh 46.5 dB attenuation

❷Implement 5-bit volume control only. Writing 1xxxxx will be interpreted as x11111 and response when read with x11111 too.

MX06 MONO_OUT Volume Default : 8000H

Bit	Type	Function
15	R/W	Mute Control 0 : Normal 1 : Mute (-∞ dB)
14:5		Reserved
4:0	R/W	Mono Master Volume (MMV[4..0]) in 1.5 dB step

❶ For MMV,
00h 0 dB attenuation
1Fh 46.5 dB attenuation

❷Implement 5-bit volume control only. Writing 1xxxxx will be interpreted as x11111 and

response when read with x11111 too.

MX0A **PC BEEP Volume** **Default : 0000H**

Bit	Type	Function
15	R/W	Mute Control 0 : Normal 1 : Mute (-∞ dB)
14:5		Reserved
4:1	R/W	PC Beep Volume (PBV[3..0]) in 3 dB step
0		Reserved

❶ For PBV,

00h 0 dB attenuation

0Fh 45 dB attenuation

MX0C **PHONE Volume** **Default : 8008H**

Bit	Type	Function
15	R/W	Mute Control 0 : Normal 1 : Mute (-∞ dB)
14:5		Reserved
4:0	R/W	Phone Volume (PV[4..0]) in 1.5 dB step

❶ For PV,

00h +12 dB Gain

08h 0dB gain

1Fh -34.5dB Gain

MX0E **MIC Volume** **Default : 8008H**

Bit	Type	Function
15	R/W	Mute Control 0 : Normal 1 : Mute (-∞ dB)
14:7		Reserved
6	R/W	20 dB boost control 0 : Normal 1: 20 dB boost
5		Reserved
4:0	R/W	Mic Volume (MV[4..0]) in 1.5 dB step

❶ For MV,

00h +12 dB Gain

08h 0dB gain

1Fh -34.5dB Gain

MX10 **LINE_IN Volume** **Default : 8808H**

Bit	Type	Function
15	R/W	Mute Control 0 : Normal 1 : Mute (-∞ dB)
14:13		Reserved
12:8	R/W	Line-In Left Volume (NLV[4..0]) in 1.5 dB step
7:5		Reserved
4:0	R/W	Line-In Right Volume (NRV[4..0]) in 1.5 dB step

❶ For NLV/NRV,

00h +12 dB Gain

08h 0dB gain

1Fh -34.5dB Gain

MX12 **CD Volume** **Default : 8808H**

Bit	Type	Function
15	R/W	Mute Control 0 : Normal 1 : Mute (-∞ dB)
14:13		Reserved
12:8	R/W	CD Left Volume (CLV[4..0]) in 1.5 dB step
7:5		Reserved
4:0	R/W	CD Right Volume (CRV[4..0]) in 1.5 dB step

❶ For CLV/CRV,

00h +12 dB Gain

08h 0dB gain

1Fh -34.5dB Gain

MX14 **VIDEO Volume** **Default : 8808H**

Bit	Type	Function

15	R/W	Mute Control 0 : Normal 1 : Mute (-∞ dB)
14:13		Reserved
12:8	R/W	Video Left Volume (VLV[4..0]) in 1.5 dB step
7:5		Reserved
4:0	R/W	Video Right Volume (VRV[4..0]) in 1.5 dB step

❶ For VLV/VRV,

00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

MX16 AUX Volume Default : 8808H

Bit	Type	Function
15	R/W	Mute Control 0 : Normal 1 : Mute (-∞ dB)
14:13		Reserved
12:8	R/W	AUX Left Volume (ALV[4..0]) in 1.5 dB step
7:5		Reserved
4:0	R/W	AUX Right Volume (ARV[4..0]) in 1.5 dB step

❶ For ALV/ARV,

00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

MX18 PCM_OUT Volume Default 8808H

Bit	Type	Function
15	R/W	Mute Control 0 : Normal 1 : Mute (-∞ dB)
14:13		Reserved
12:8	R/W	PCM Volume (PLV[4..0]) in 1.5 dB step
7:5		Reserved
4:0	R/W	PCM Right Volume (PRV[4..0]) in 1.5 dB step

❶ For PLV/PRV,

00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

MX1A Record Select Default : 0000H

Bit	Type	Function
15:11		Reserved
10:8	R/W	Left record source select (LRS[2..0])
7:3		Reserved
2:0	R/W	Right record source select (RRS[2..0])

❶ For LRS

0 MIC
1 CD LEFT
2 VIDEO LEFT
3 AUX LEFT
4 LINE LEFT
5 STEREO MIXER OUTPUT LEFT
6 MONO MIXER OUTPUT
7 PHONE

❷ For RRS

0 MIC
1 CD RIGHT
2 VIDEO RIGHT
3 AUX RIGHT
4 LINE RIGHT
5 STEREO MIXER OUTPUT RIGHT
6 MONO MIXER OUTPUT
7 PHONE

MX1C Record Gain Default : 8000H

Bit	Type	Function
15	R/W	Mute Control 0 : Normal 1 : Mute (-∞ dB)
14:12		Reserved
11:8	R/W	Left Record Gain Select (LRG[3..0]) in 1.5 dB step
7:4		Reserved
3:0	R/W	Right Record Gain Select (RRG[3..0]) in 1.5 dB step

❶ For LRG/RRG

0Fh +22.5dB

00h 0 dB (No Gain)

MX20 General Purpose Register Default : 0000H

Bit	Type	Function
15	R/W	PCM output path 0 : pre 3D 1 : post 3D
14		Reserved, Read as 0
13	R/W	3D Control 1 : On 0 : Off
12:10		Reserved, Read as 0
9	R/W	Mono output select 0 : MIX 1 : MIC
8	R/W	Mic select 0 : Mic 1 1 : Mic 2
7	R/W	AD to DA loop-back control 0 : Disable 1 : Enable
6:0		Reserved

MX22 3D Control Default : 0000H

Bit	Type	Function
15: 2		Reserved ,Read as 0
1:0	R/W	Depth control (DP[1..0])

❶3D effect control

DP[1..0]	Function
00	Off (R=0KΩ)
01	33% (R=5KΩ)
10	66%(R=7.5KΩ)
11	100%(R=10KΩ)

In our design,3D block output is enabled only when (MX20.13=1)

MX26 Powerdown Control/Status Default : 0000H

Bit	Type	Function
15	R/W	External Amplifier Power Down (EAPD) 0 : normal 1 : Power down
14		Reserved
13	R/W	PR5 0 : Normal 1 : Disable internal clock
12	R/W	PR4 0 : Normal 1 : Power down AC-Link
11	R/W	PR3 0 : Normal 1 : Power down Mixer (Vref off)
10	R/W	PR2 0 : Normal 1 : Power down Mixer (Vref still on)
9	R/W	PR1 0 : Normal 1 : Power down PCM DAC
8	R/W	PR0 0 : Normal 1 : Power down PCM ADC and input MUX
7:4		Reserved, Read as 0
3	R	Vref status 1 : Vref is up to normal level 0 : Not yet
2	R	Analog Mixer status 1 : Ready 0 : Not yet
1	R	DAC status 1 : Ready 0 : Not yet
0	R	ADC status 1 : Ready 0 : Not yet

MX28 Extended Audio ID Default : 0200H

Bit	Type	Function
15	R	ID1
14	R	ID0
13:10		Reserved, Read as 0
9	R	AMAP read as 1 (DAC mapping base on Codec ID)
8:0		Reserved, Read as 0

❶ID1 is latched inversely from pin 46 when system reset. ID0 is latched inversely from pin 45 when system reset.

❷ALC100 map DAC slot according to the following table

ID[1..0]	PCM Left DAC slot #	PCM Right DAC slot #	Comment
00	3	4	Primary
01	3	4	Secondary (Docking)
10	7	8	Secondary (Surround)
11	6	9	Secondary (Center/LFE)

MX72 Extension control register 2 Default : 1199H

Bit	Type	Function
15:14		Reserved
13:12	R/W	ADDA bias current 00 : 10uA 01 : 20uA 10 : 30uA 11 : 40uA
11:10		Reserved
9:8	R/W	Vref bias current 00 : 10uA 01 : 20uA 10 : 30uA 11 : 40uA
7:6	R/W	VBG control
5:4	R/W	VAG control 00 : 2V 01 : 2.2V 10 : 2.4V 11 : 2.6V
3:2	R/W	(Vrefp-Vrefn) control 00 : 0.4VAG others : 0.5VAG
1:0	R/W	Mixer bias current 00 : 5uA 01 : 10uA 10 : 15uA 11 : 20uA

❶For version latter than B, bit 3~2 are dummy and the select is always 0.5VAG.

MX7C VENDOR ID1 Default : 414CH

Bit	Type	Function
15:0	R	Vendor ID "AL"

MX7E VENDOR ID2 Default : 432XH

Bit	Type	Function
15:8	R	Vendor ID "C"
7:4	R	Chip ID 0010
3:0	R	Version number 00 : version A

❶Chip ID 0010 RL5383/RL5522

5. Design Suggestion :

5.1 Clocking :

The clock source of different configuration is listed below :

CODEC ID[1..0]	BIT-CLK	Clock source
00	**Output**	Crystal or external clock (XTAL-IN)
01	**Input**	external clock (XTAL-IN)
10	**Input**	external clock (XTAL-IN)
11	**Input**	external clock (XTAL-IN)

5.2 AC-Link :

When ALC100 take serial data from AC97 controller, it sample **SDATA_OUT** on the falling edge of **BIT_CLK** .When ALC100 send serial data to AC97 controller, it start to drive **SDATA_IN** on the rising edge of **BIT_CLK.**

ALC100 will return any uninstalled bits or registers with 0 for read operation.. ALC100 also stuff the unimplemented slot or bit with 0 in **SDATA-IN**. Note that AC-LINK is MSB-justified.

Refer to "*Audio CODEC '97 Component Specification Revision 2.1"* for detail.

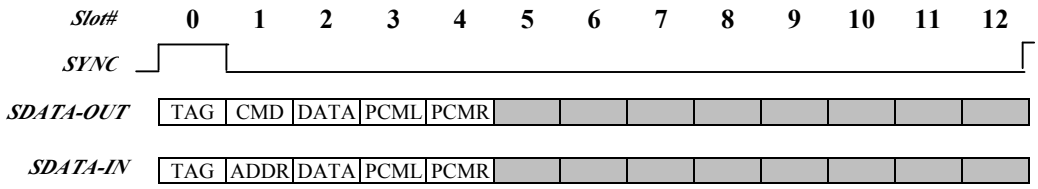


Fig5.2-1 ALC100 slot arrangement – CODEC ID = 00 or 01

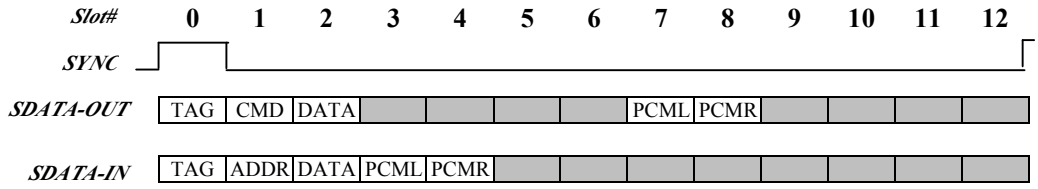


Fig5.2-2 ALC100 slot arrangement – CODEC ID = 10

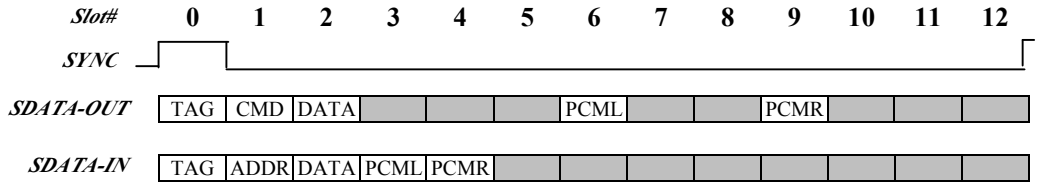


Fig5.2-3 ALC100 slot arrangement – CODEC ID = 11

5.3 Reset :

There are 3 kinds of reset operation. ***Cold, Warm*** and ***Register*** reset which listed below :

Reset Type	Trigger condition	CODEC response
Cold	Assert RESET# for a specified period	Reset all hardware logic and all registers to it' s default value.
Register	Write register indexed 00h	Reset all registers to it' s default value.
Warm	Driven SYNC high for specified period without BIT_CLK	Reactivates AC-LINK, no change to register values.

The AC97 controller should drive SYNC and SDATA-OUT low during the period of RESET# assertion to guarantee ALC100 reset successfully.

5.4 CD Input :

Pay attention to differential CD input. Below is an example of differential CD input.

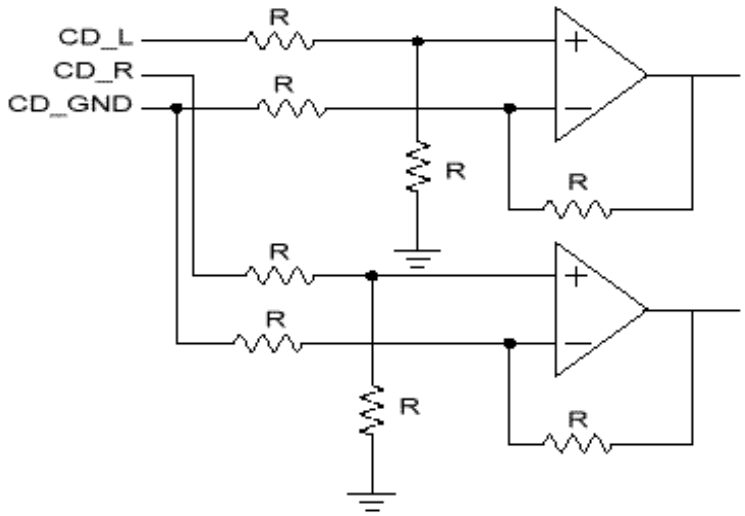


Fig 5.4-1 Example of differential CD input

5.5 Odd Addressed Register Access :

ALC100 will not response to odd-addressed register access for future compatibility.

5.6 Power-down Mode :

Pay special attention to powerdown control register (index 26h),expecially PR4 (powerdown AC-link).

5.7 Test Mode :

5.7.1 ATE In Circuit Test Mode :

SDATA_OUT is sampled high at the trailing edge of **RESET#.** at this mode ALC100 will drive **BIT_CLK**
and **SDATA_IN** to high impedance state.

5.7.2 Vendor Specific Test Mode :

SYNC is sampled high at the trailing edge of **RESET#.**

6. Electrical Characteristics :

6.1 DC Characteristics :

Dvdd= 5.0V or 3.3V±5%, $T_{ambient}$=25^{0}C, with 50pF external load.

Parameter	Symbol	Min	Typ	Max	Units
Input voltage range	V_{in}	-0.30	-	Dvdd+0.30	V
Low level input voltage	V_{il}	-	-	0.35Dvdd	V
High level input voltage	V_{ih}	0.4DVdd	-	-	V
High level output voltage	V_{oh}	0.5DVdd	-	-	V
Low level output voltage	V_{ol}	-	-	0.2DVdd	V
Input leakage current	-	-10	-	10	uA
Output leakage current (Hi-Z)	-	-10	-	10	uA
Output buffer drive current	-	-	5	-	mA

6.2 AC Timing Characteristics :

6.2.1 Cold Reset :

Parameter	Symbol	Min	Typ	Max	Units
RESET# active low pulse width	T_{rst_low}	1.0	-	-	us
RESET# inactive to BIT_CLK startup delay	$T_{rst2clk}$	162.8	-	-	ns

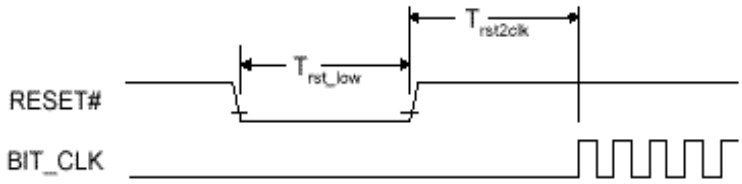


Fig 6.2.1-1 Cold reset timing diagram

6.2.2 Warm Reset :

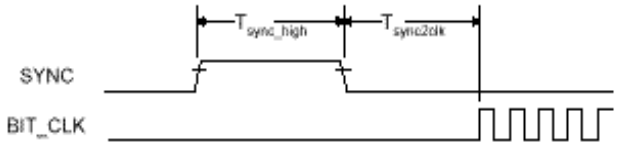


Fig 6.2.2-1 Cold reset timing diagram

Parameter	Symbol	Min	Typ	Max	Units
SYNC active high pulse width	T_{sync_high}	1.0	-	-	us
SYNC inactive to BIT_CLK Startup delay	$T_{sync2clk}$	162.8	-	-	ns

6.2.3 AC-Link Clocks :

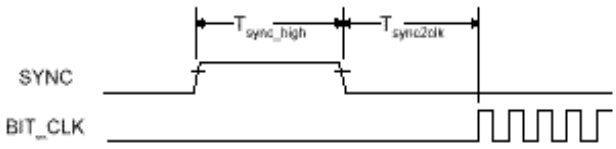


Fig 6.2.3-1 BIT_CLK and SYNC timing diagram

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	T_{clk_period}	-	81.4	-	ns
BIT_CLK output jitter		-	-	750	ps
BIT_CLK high pulse width (note 2)	T_{clk_high}	36	40.7	45	ns
BIT_CLK low pulse width (note 2)	T_{clk_low}	36	40.7	45	ns
SYNC frequency		-	48.0	-	KHz
SYNC period	T_{sync_period}	-	20.8	-	us
SYNC high pulse width	T_{sync_high}	-	1.3	-	us
SYNC low pulse width	T_{sync_low}	-	19.5	-	us
Note 1 : 47.5~70pF **********					
Note 2 : Worse case duty cycle restricted to 45/55.					

6.2.4 Data Output and Input Times :

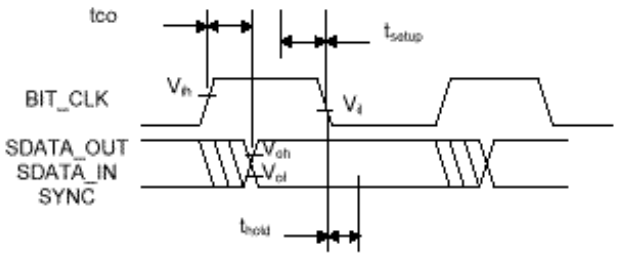


Fig 6.2.4-1 Data Output and Input timing diagram

Parameter	Symbol	Min	Typ	Max	Units
Output Valid Delay from rising edge of BIT_CLK	t_{co}	-	-	15	ns
Note 1 : Timing is for SDATA and SYNC outputs with respect to BIT_CLK *at the device driving the output.* Note 2 : 50pF external load					

Parameter	Symbol	Min	Typ	Max	Units
Input Setup to falling edge of BIT_CLK	t_{setup}	10	-	-	ns
Input Hold from falling edge of BIT_CLK	t_{hold}	10	-	-	ns
Note : Timing is for SDATA and SYNC outputs with respect to BIT_CLK *at the device driving the output.*					

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK combined rise or fall plus flight time		-	-	7	ns
SDATA combined rise or fall plus flight time		-	-	7	ns
Note : Combined rise or fall plus flight times are provided for worst case scenario modeling purpose.					

6.2.5 Signal Rise and Fall Times :

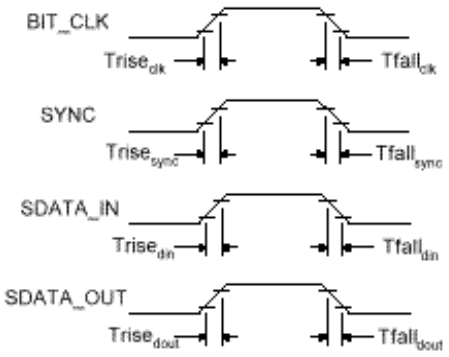


Fig 6.2.5-1 Signal Rise and Fall timing diagram

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK rise time	$Trise_{clk}$	2	-	6	ns
BIT_CLK fall time	$Tfall_{clk}$	2	-	6	ns
SYNC rise time	$Trise_{sync}$	2	-	6	ns
SYNC fall time	$Tfall_{sync}$	2	-	6	ns
SDATA_IN rise time	$Trise_{din}$	2	-	6	ns
SDATA_IN fall time	$Tfall_{din}$	2	-	6	ns
SDATA_OUT rise time	$Trise_{dout}$	2	-	6	ns
SDATA_OUT fall time	$Tfall_{dout}$	2	-	6	ns

Note 1 : 50pF external load Note 2 : rise is from 10% to 90% of Vdd (V_{ol} to V_{oh}) Note 3 : fall is from 90% to 10% of Vdd (V_{oh} to V_{ol})

6.2.6 AC-Link Low Power Mode Timing :

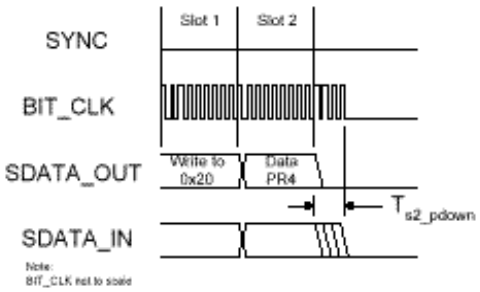


Fig 6.2.6-1 AC-Link low power mode timing diagram

Parameter	Symbol	Min	Typ	Max	Units
End of slot 2 to BIT_CLK, SDATA_IN low	T_{s2_pdown}	-	-	1.0	us

6.2.7 ATE Test Mode :

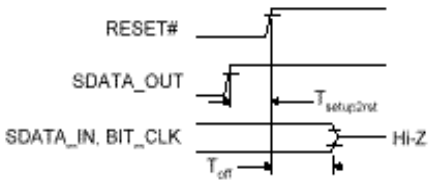


Fig 6.2.6-1 ATE test mode timing diagram

Parameter	Symbol	Min	Typ	Max	Units
Setup to trailing edge of RESET# (also applies to SYNC)	$T_{setup2rst}$	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	T_{off}	-	-	25.0	ns

6.2.8 AC-Link IO Pin Capacitance and Loading :

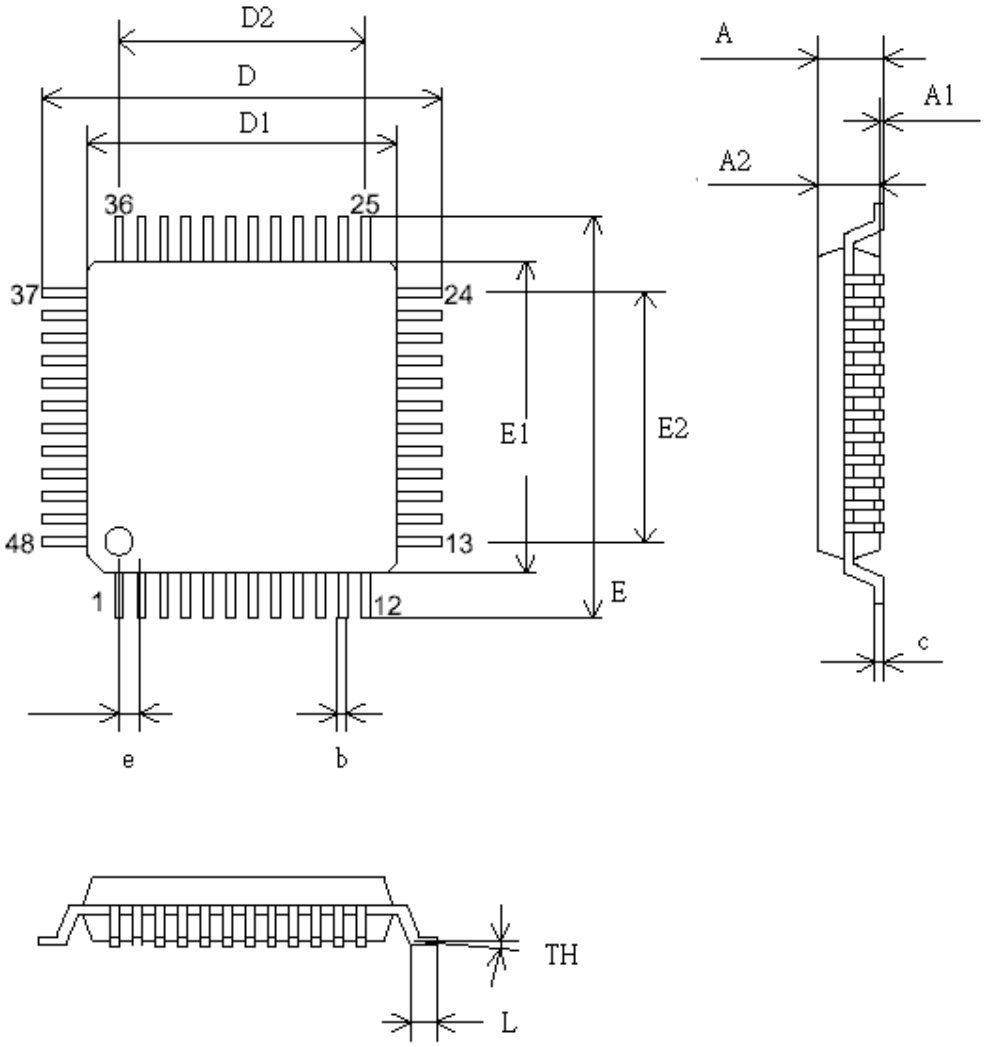
Output Pin	1 Codec	2 Codec	3 Codec	4 Codec
BIT_CLK (must support ≥ 2 Codecs)	55pF	55pF	62pF	70pF
SDATA_IN	47.5pF	47.5pF	47.5pF	47.5pF

7. Analog Performance Characteristics :

Standard test condition : $T_{ambient}=25^0C$, Dvdd=5.0 or 3.3V ±5%,Avdd=5.0V±5%
Input Voltage Level : Logic Low=0.35*Vdd, Logic High=0.65Vdd
1KHz input sine wave; Sampling frequency=48KHz; 0dB=1Vrms
10KΩ/50pF load; Testbench Characterization BW :20Hz~20KHz
0dB attenuation; tone and 3D disabled

Parameter	Min	Typ	Max	Units
Full scale input voltage				
Line inputs	-	1.0	-	Vrms
Mic inputs	-	0.1	-	
Full scale output voltage				
Line output	-	1.0	-	Vrms
Analog S/N				
CD to LINE_OUT	90	-	-	dB
Other to LINE_OUT	-	85	-	
Analog frequency response	20	-	20,000	Hz
Digital S/N				
D/A	85	90	-	dB
A/D	80	85	-	
Total Harmonic Distortion				
Line output	-	-	0.02	%
D/A & A/D frequency response	20	-	19,200	Hz
Transition Band	19,200	-	28,800	Hz
Stop Band	28,800	-	∞	Hz
Stop Band Rejection	-74	-	-	dB
Out-of-Band Rejection	-	-40	-	dB
Group delay	-	-	1	ms
Power supply rejection ratio (1KHz)	-	-40	-	dB
Crosstalk between inputs channels	-	-	-70	dB
Spurious Tone Reduction	-	-100	-	dB
Attenuation, Gain Step Size	-	1.5	0	dB
Input impedance	10	40	-	KΩ
Input Capacitance	-	7.5	-	pF
V_{refout}	-	2.25-2.75	-	V

8. Package:



SYMBOL	MILLIMETER			INCH		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
c	0.09		0.20	0.004		0.008
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
D2	5.50			0.217		
E	9.00 BSC			0.354 BSC		
E1	7.00BSC			0.276 BSC		
E2	5.50			0.217		
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC			0.016 BSC		
TH	0^o	3.5^o	7^o	0^o	3.5^o	7^o
L	0.45	0.60	0.75	0.018	0.024	0.030