High Definition Audio SoundMAX Codec

AD1987

FEATURES

3 stereo headphones
Microsoft Vista Premium logo for desktop
95 dB audio outputs, 90 dB audio inputs
Internal 32-bit arithmetic for greater accuracy
Impedance and presence detection on all jacks
Retaskable jacks
4 independent microphone bias pins
Digital and analog PCBeep
C/LFE channel swapping
2 general-purpose digital I/O (GPIO) pins
Advanced power management modes
48-lead LFCSP_VQ package

EIGHT 192 kHz DACs

4 independent stereo DAC pairs
7.1 surround sound or 5.1 stereo out plus independent headphone
Independent 8 kHz, 11.025 kHz, 16 kHz, 22.05 kHz, 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz sample rates
16-, 20-, and 24-bit PCM resolution
Selectable stereo mixer on outputs

FOUR 96 kHz ADCs

2 independent stereo ADC pairs
Simultaneous record of up to 4 channels
Independent 8 kHz, 11.025 kHz, 16 kHz, 22.05 kHz, 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, and 96 kHz sample rates
16-, 20-, and 24-bit PCM resolution
Support for quad microphone arrays

S/PDIF OUTPUT

Supports 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz sample rates
16-, 20-, and 24-bit data; PCM, AC3
Digital PCM gain control

DEDICATED AUXILIARY PINS

Stereo CD/auxiliary I/O port w/GND sense
Mono out pin for internal speakers or telephony

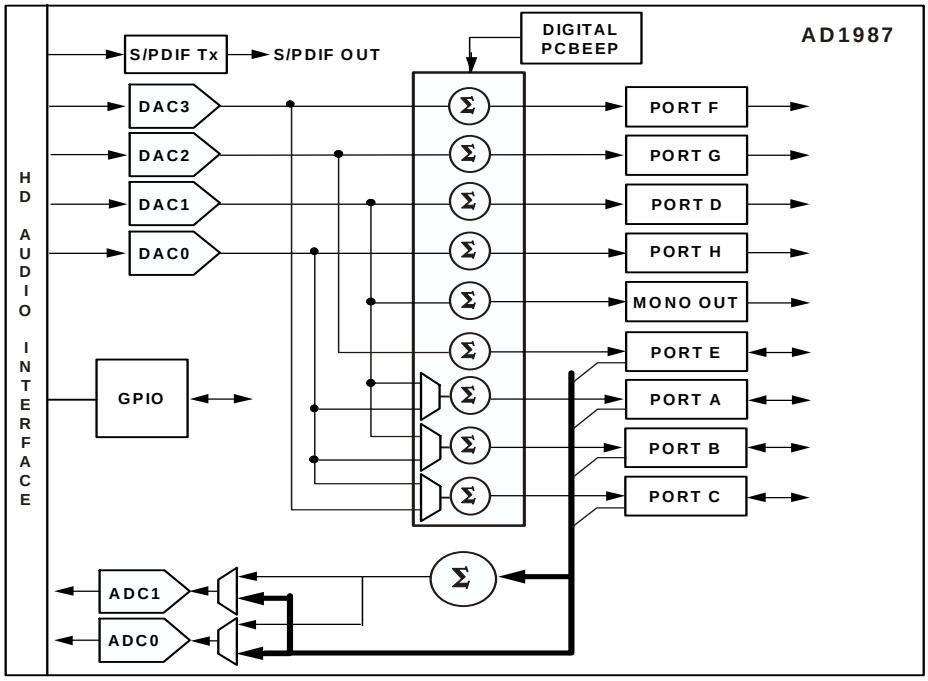

Figure 1. AD1987 Block Diagram

Rev. A

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GENERAL DESCRIPTION

The AD1987 audio codec and SoundMAX® software provides superior HD audio quality that exceeds Vista Premium performance. The AD1987 has eight DACs and four ADCs, three stereo headphone ports, C/LFE swapping, digital and analog PCBeep, and S/PDIF output, making the AD1987 the right choice for desktop PCs where performance is the primary consideration.

The jack retasking feature on this product supports various configurations including platforms for 7.1 on 5 jacks, 5.1 on 3 jacks, and front panel jack retasking.

The AD1987 is available in a 48-lead Pb-free frame chip scale package in both reels and trays. See Ordering Guide on Page 17.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the AD1987 SoundMAX codec's architecture and functionality. Additional information on the AD1987 is available in the AD1987 Programmers Reference Manual. Please contact your local Analog Devices Inc. sales representative for more information. For information on SoundMAX codecs and software, see Analog Devices website at http://www.analog.com/soundMAX.

JACK CONFIGURATION

The guidelines shown in Table 1 through Table 3 should be used when selecting ports for particular functions. The symbols used in this table are defined as: LI = line level input, LO = line level output, HP = output capable of driving headphone load, MIC = input supports microphones with MIC bias and boost amplifier.

Table 1. Desktop Applications with Discrete Jacks (Default Configuration)

Port	HP	MIC	LO	LI
Port A – Front Panel Headphone	x	x	x	x
Port B – Front Panel Microphone	x	x	x	x
Port C – Rear Panel Line-In		x	x	x
Port D – Rear Panel Front/Headphone	x		x	x
Port E – Rear Panel Microphone		x	x	x
Port F – Rear Panel Surround-Rear (5.1)			x	
Port G – Rear Panel C/LFE			x	
Port H – Rear Panel Surround-Center/Side (7.1)			x	

Table 2. Retasking to Support 7.1 Audio on 5 Jacks

Port	HP	MIC	LO	LI
Port A – Front Panel Headphone	x	x	x	x
Port B – Front Panel Microphone	x	x	x	x
Port C – Rear Panel Line-In/Surround-Center/Side (7.1)		x	x	x
Port D – Rear Panel Front/Headphone	x		x	x
Port E – Rear Panel Microphone		x	x	x
Port F – Rear Panel Surround-Rear (5.1)			x	
Port G – Rear Panel C/LFE			x	

Table 3. Desktop Applications with Retasking to Support 5.1 Audio on 3 Jacks

Port	HP	MIC	LO	LI
Port A – Front Panel Headphone	x	x	x	x
Port B – Front Panel Microphone	x	x	x	x
Port C – Rear Panel Line-In/Surround-Rear (5.1)		x	x	x
Port D – Rear Panel Front/Headphone	x		x	x
Port E – Rear Panel Microphone /C/LFE		x	x	x

SPECIFICATIONS

TEST CONDITIONS

Parameter	Test Condition
Temperature	25°C
Digital Supply	3.3 V
Analog Supply	3.3 V
MIC_BIAS_IN (via Low-Pass Filter)	5.0 V
Sample Rate f_S	48 kHz
Input Signal (Frequency Sine Wave)	1008 Hz
Amplitude for THD + N	–3.0 dB Full Scale
Analog Output Pass Band	20 Hz to 20 kHz
DAC	10 kΩ Output Load: Line Out Tests
	32 Ω Output Load: Headphone Tests
ADC	0 dB Gain

PERFORMANCE

Parameter	Min	Typ	Max	Unit
Line Out Drive (10 kΩ loads—DAC to Pin)				
Total Harmonic Distortion (THD + N)		–85		dB
Dynamic Range (–60 dB in ref to f_S A-Weighted)		95		dB
Signal-to-Noise Ratio		95		dB
Headphone Drive (32 Ω loads—DAC to Pin)				
Total Harmonic Distortion (THD + N)		–83		dB
Dynamic Range (–60 dB in ref to f_S A-Weighted)		95		dB
Signal-to-Noise Ratio		95		dB
Input Ports (Mic Boost = 0 dB)				
Total Harmonic Distortion (THD + N)		–81		dB
Dynamic Range (–60 dB in ref to f_S A-Weighted)		90		dB
Signal-to-Noise Ratio		90		dB

GENERAL SPECIFICATIONS

Parameter	Min	Typ	Max	Unit
DIGITAL DECIMATION AND INTERPOLATION FILTERS[1]—f_S = 8 kHz to 192 kHz				
Pass Band	0		0.4 f_S	Hz
Pass-Band Ripple			±0.005	dB
Stop Band	0.6 f_S			Hz
Stop-Band Rejection			–100	dB
Group Delay		20		$1/f_S$
Group Delay Variation Over Pass Band		0		µs
ANALOG-TO-DIGITAL CONVERTERS				
Resolution		24		Bits
Gain Error (Full-Scale Span Relative to Nominal Input Voltage)[2]			±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)		±0.2	±0.5	dB
ADC Offset Error[1]			±5	mV
ADC Crosstalk[1]				
Line Inputs (Input L, Ground R, Read R; Input R, Ground L, Read L)		–85		dB
Line_In to Other		–100	–80	dB

Parameter		Min	Typ	Max	Unit
DIGITAL-TO-ANALOG CONVERTERS					
Resolution			24		Bits
Gain Error (Full-Scale Span Relative to Nominal Input Voltage)[1]				±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)				±0.5	dB
Total Audible Out-of-Band Energy (Measured from 0.6 × f_S to 20 kHz)[1]			–85		dB
DAC Crosstalk (Input L, Zero R, Measure R_OUT; Input R, Zero L, Measure L_OUT)[1]			–95		dB
DAC VOLUMES					
Step Size (DAC-0, DAC-1, DAC-2, DAC-3)			1.5		dB
Output Gain/Attenuation Range		–58.5		0	dB
Mute Attenuation of 0 dB Fundamental[1]			–80		dB
ADC VOLUMES					
Step Size (ADCSEL-0, ADCSEL-1)			1.5		dB
PGA Gain/Attenuation Range		–58.5		+22.5	dB
ANALOG MIXER					
Signal-to-Noise Ratio Input to Output—Ports B, C, or F, to Port D Output			95		dB
Step Size: All Mixer Inputs			–1.5		dB
Input Gain/Attenuation Range: All Mixer Inputs		–34.5		+12.0	dB
ANALOG LINE LEVEL OUTPUTS					
Full-Scale Output Voltage: Line out drive enabled		1.0			V rms[3]
Ports A, D, E, F, and Mono Out		2.83			V p-p
	Output Impedance[1]		190		Ω
	External Load Impedance[1]	10			kΩ
	Output Capacitance[1]		15		pF
	External Load Capacitance[1]			1000	pF
ANALOG HP DRIVE OUTPUTS					
Full-Scale Output Voltage: Line Out Drive Enabled		1.0			V rms[3]
Ports A and D (when HP Drive is Enabled)		2.83			V p-p
	Output Impedance[1]			0.5	Ω
	External Load Impedance[1]	32			Ω
	Output Capacitance[1]		15		pF
	External Load Capacitance[1]			1000	pF
ANALOG INPUTS					
Input Voltages—Ports B, C, or E					
	Mic Boost = 0 dB		1		V rms[3]
			2.83		V p-p
Input Voltages—Microphone Boost	Mic Boost = +10 dB		0.316		V rms[3]
Amplifier, Ports B, C, or E			0.894		V p-p
	Mic Boost = +20 dB		0.1		V rms[3]
			0.283		V p-p
	Mic Boost = +30 dB		0.032		V rms[3]
			0.089		V p-p
Input Impedance					
PCBEEP			23		kΩ
Ports B, C, E (Mic Boost = 0 dB)			150		kΩ
Port F			45		kΩ
Input Capacitance[1]			5	7.5	pF

Parameter		Min	Typ	Max	Unit
MICROPHONE BIAS					
MIC_BIAS-B, MIC_BIAS-C					
MIC_BIAS_IN (Pin 33) = +5 V or +3.3 V	V_{REF} Setting = High-Z		High-Z		
	V_{REF} Setting = 0 V		0		V dc
	V_{REF} Setting = 50%		1.65		V dc
MIC_BIAS_IN (Pin 33) = +5 V	V_{REF} Setting = 80%		3.7		V dc
	V_{REF} Setting = 100%		3.9		V dc
MIC_BIAS_IN (Pin 33) = +3.3 V	V_{REF} Setting = 80%		2.86		V dc
	V_{REF} Setting = 100%		3.0		V dc
MIC_BIAS-E (When enabled as BIAS)	V_{REF} Setting = High-Z		High-Z		V dc
	V_{REF} Setting = 0 V		0		V dc
	V_{REF} Setting = 50%		1.65		V dc
	V_{REF} Setting = 80%		2.86		V dc
	V_{REF} Setting = 100%		3.0		V dc
Output Drive Current	V_{REF} Setting = 50%, 80%, or 100%		1.6		mA
GPIO 0 and GPIO 1					
Input Signal High (V_{IH})		$DV_{IO} \times 0.60$		DV_{IO}	V
Input Signal Low (V_{IL})		0		$DV_{IO} \times 0.24$	V
Output Signal High (V_{OH})	I_{OUT} = –500 µA	$DV_{IO} \times 0.72$		DV_{IO}	V
Output Signal Low (V_{OL})	I_{OUT} = +1500 µA	0		$DV_{IO} \times 0.10$	V
Input Leakage Current (Signal High) (I_{IH})			–150		µA
Input Leakage Current (Signal Low) (I_{IL})			–50		µA
POWER SUPPLY					
Analog (AV_{DD}) 3.3 V ± 5%					
Power Supply Range		3.13	3.30	3.46	V
Power Dissipation			135		mW
Supply Current			41		mA
Digital (DV_{DD}) 3.3 V ± 10%					
Power Supply Range		2.97	3.30	3.63	V
Power Dissipation			218		mW
Supply Current			66		mA
Digital I/O (DV_{IO}) 3.3 V ± 10%					
Power Supply Range		2.97	3.30	3.63	V
Power Dissipation			3.96		mW
Supply Current			1.20		mA
Power Supply Rejection (Reference to f_S 100 mV p-p Signal @ 1 kHz)[1]			80		dB

[1] Guaranteed but not tested.
[2] Measurements reflect main ADC.
[3] RMS values assume sine wave input.

HD AUDIO LINK SPECIFICATION

HD Audio signals comply with the High Definition Audio Specifications. Please refer to these specifications at:
http://www.intel.com/standards/hdaudio/

POWER-DOWN STATES

Parameter	ID_{VDD} Typ	IA_{VDD} Typ	Unit
Function Node in D0, All Nodes Active	66	41	mA
Function Node in D3	21	1.2	mA
Codec in $\overline{\text{RESET}}$	3	3	mA
Individual Block Power Savings			
DAC Pair Powered Down Saves (Each)	6	5	mA
ADC Pair Powered Down Saves (Each)	5.3	3.2	mA
Mixer Power Control (And Associated Amps) Saves	0	2	mA
MIC_BIAS Powered Down Saves[1, 2]	0	0.5	mA

[1] Powering down the MIC_BIAS powers down all port MIC_BIAS pins. This disables all microphone bias circuits set to 100% or 50%, setting them to the high-Z state. The 0 Ω and high-Z states remain unaffected by the MIC_BIAS power state.

[2] Test conditions: 30 pF load, 2.0 MHz frequency, 3.3 V A_{VDD}.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed below may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Power Supplies	Rating
Digital (DV_{DD})	–0.30 V to +3.65 V
Digital I/O (DV_{IO})	–0.30 V to +3.65 V
Analog (AV_{DD})	–0.30 V to +3.65 V
Input Current (except supply pins)	±10.0 mA
Analog Input Voltage (Signal Pins)	–0.30 V to AV_{DD} +0.3 V
Digital Input Voltage (Signal Pins)	–0.30 V to DV_{IO} +0.3 V
Ambient Temperature (Operating)	0°C to +70°C
Storage Temperature	–65°C to +150°C

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating

$T_{AMB} = T_{CASE} – (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W
θ_{CA} = Thermal Resistance (Case-to-Ambient)
θ_{JA} = Thermal Resistance (Junction-to-Ambient)
θ_{JC} = Thermal Resistance (Junction-to-Case)

All measurements per EIA-JESD51 with 2S2P test board per EIA-JESD51-7.

Table 4. Thermal Resistance

Package	θ_{JA}	θ_{JC}	θ_{CA}	Unit
LFCSP_VQ	97	15	32	°C/W

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

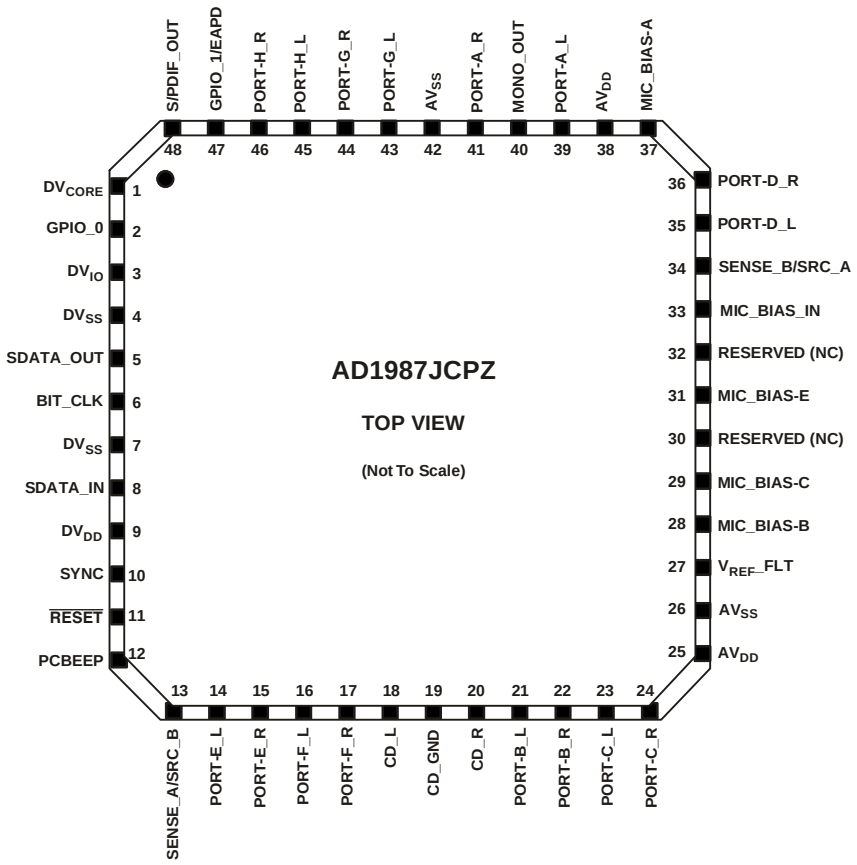

Figure 2. AD1987 48-Lead Package and Pinout

Table 5. AD1987 Pin Descriptions

Mnemonic	Pin No.	Function	Description
DIGITAL INTERFACE			
SDATA_OUT	5	I	Link Serial Data Output. Clocked on both edges of BIT_CLK.
BIT_CLK	6	I	Link Bit Clock. 24.000 MHz serial data clock.
SDATA_IN	8	I/O	Link Serial Data Input. AD1987 output stream clocked only on one edge of BIT_CLK.
SYNC	10	I	Link Frame Sync.
$\overline{\text{RESET}}$	11	I	Link Reset. Master hardware reset.
DIGITAL I/O			
GPIO_0	2	I/O	General-Purpose Input/Output Pin. Digital signal used to control external circuitry.
GPIO_1/EAPD	47	I/O	General-Purpose Input/Output Pin/EAPD Pin. Digital signal used to control external circuitry. By default pin is in a high-Z state. When used as EAPD: high-Z = amp on, DV_{SS} = amp off.
S/PDIF_OUT	48	O	S/PDIF_OUT. Supports S/PDIF output.
JACK SENSE			
SENSE_A/SRC_B	13	I/O	JACK Sense A-D Input/Sense B Drive.
SENSE_B/SRC_A	34	I/O	JACK Sense E-H Input/Sense A Drive.
ANALOG I/O			
PCBEEP	12	LI	Monaural Input From System for Analog PCBeep.
PORT-E_L	14	LI, MIC, LO, SWAP	Auxiliary Input/Output Left Channel.
PORT-E_R	15	LI, MIC, LO, SWAP	Auxiliary Input/Output Right Channel.
PORT-F_L	16	LO	Auxiliary Input/Output Left Channel.
PORT-F_R	17	LO	Auxiliary Input/Output Right Channel.
CD_L	18	LI	CD Audio Left Channel.
CD_GND	19	LI	CD-Audio-Analog-Ground-Reference (for Differential CD Input). Must be connected to AGND via 0.1 μF capacitor if not in use as CD_GND.
CD_R	20	LI	CD Audio Right Channel.
PORT-B_L	21	LI, MIC, HP, LO	Front Panel Stereo MIC/Line-In.
PORT-B_R	22	LI, MIC, HP, LO	Front Panel Stereo MIC/Line-In.
PORT-C_L	23	LI, MIC, LO	Rear Panel Stereo MIC/Line-In.
PORT-C_R	24	LI, MIC, LO	Rear Panel Stereo MIC/Line-In.
PORT-D_L	35	LI, HP, LO	Rear Panel Headphone/Line-Out.
PORT-D_R	36	LI, HP, LO	Rear Panel Headphone/Line-Out.
PORT-A_L	39	LI, MIC, HP, LO	Front Panel Headphone/Line-Out.
MONO_OUT	40	LO	Monaural Output to Internal Speaker or Telephony Subsystem Speakerphone.
PORT-A_R	41	LI, MIC, HP, LO	Front Panel Headphone/Line-Out.
PORT-G_L	43	LO, SWAP	Rear Panel C/LFE Output.
PORT-G_R	44	LO, SWAP	Rear Panel C/LFE Output.
PORT-H_L	45	LO	Rear Panel Surround Center/Side.
PORT-H_R	46	LO	Rear Panel Surround Center/Side.
FILTER/REFERENCE			
MIC_BIAS-B	28	O	Switchable Microphone Bias. For use with Port B (Pins 21, 22).
MIC_BIAS-C	29	O	Switchable Microphone Bias. For use with Port C (Pins 23, 24).
MIC_BIAS-E	31	O	Switchable Microphone Bias. For use with Port E (Pins 14, 15).
V_{REF}_FLT	27	O	Voltage Reference Filter.
MIC_BIAS-A	37	O	Switchable Microphone Bias. For use with Port A (Pins 39, 41)
			All MIC_BIAS pins are capable of:
			High-Z, 0 V, 1.65 V, 3.78 V, and 3.95 V (with 5.0 V on Pin 33)
			High-Z, 0 V, 1.65 V, 2.86 V, and 3.00 V (with 3.3 V on Pin 33).
DV_{CORE}	1	O	CAUTION: DO NOT APPLY 3.3 V TO THIS PIN!
			Filter connection for internal core voltage regulator.
			This pin must be connected to filter caps: 10 μF, 1.0 μF, and 0.1 μF connected in parallel between Pin 1 and DV_{SS} (Pin 4).

The symbols used in this table are defined as: I = Input, O = Output, LI = Line level input, LO = Line level output, HP = Output capable of driving headphone load, MIC = Input supports microphones with MIC bias and boost amplifier, SWAP = Outputs can swap L/R channels (typically used to support C/LFE or shared C/LFE function).

Table 5. AD1987 Pin Descriptions (Continued)

Mnemonic	Pin No.	Function	Description
POWER AND GROUND			
DV_{IO} 3.3 V ±10%	3	I	Digital Supply I/O. Connect to the I/O voltage used for the HD audio controller signals.
DV_{SS}	4, 7	I	Digital Supply Return (Ground).
DV_{DD} 3.3 V ±10%	9	I	Digital Supply Voltage 3.3 V. This is regulated down to Pin 1 to supply the internal digital core.
AV_{DD} 3.3 V ±5%	25, 38	I	CAUTION: DO NOT APPLY 5.0 V TO THESE PINS! Analog Supply Voltage 3.3 V ONLY. Note: AV_{DD} supplies should be well regulated and filtered as supply noise degrades audio performance.
MIC_BIAS_IN	33	I	Source for Microphone Bias Boost Circuitry. Connect this pin to 5.0 V via a low-pass filter. When connected this way, the AD1987 is capable of providing +3.95 V as a mic bias to all of the mic bias pins. If 5 V is not available, connect this pin to +3.3 V (AV_{DD}) via a low-pass filter. The AD1987 produces a mic bias voltage relative to the AV_{DD} supply (typically 3.0 V @ AV_{DD} = 3.3 V).
AV_{SS}	26, 42	I	Analog Supply Return (Ground). AV_{SS} should be connected to DV_{SS} using a conductive trace under, or close to, the AD1987.

The symbols used in this table are defined as: I = Input, O = Output, LI = Line level input, LO = Line level output, HP = Output capable of driving headphone load, MIC = Input supports microphones with MIC bias and boost amplifier, SWAP = Outputs can swap L/R channels (typically used to support C/LFE or shared C/LFE function).

HD AUDIO WIDGETS

In the following table, node IDs that are not shown are reserved for future use.

Node ID	Name	Type ID	Type	Description
00	ROOT	x	Root	Device identification
01	FUNCTION	x	Function	Designates this device as an audio codec
02	S/PDIF DAC	0	Audio Output	S/PDIF digital stream output interface
03	DAC_0	0	Audio Output	Headphone/surround side (7.1) channel digital/audio converters
04	DAC_1	0	Audio Output	Stereo front channel digital/audio converters
05	DAC_2	0	Audio Output	Stereo C/LFE channel digital/audio converters
06	DAC_3	0	Audio Output	Stereo surround-back (5.1) channel digital/audio converters
08	ADC_0	1	Audio Input	Stereo record Channel 1 audio/digital converters
09	ADC_1	1	Audio Input	Stereo record Channel 2 audio/digital converters
0B	S/PDIF Mix Selector	3	Audio Selector	Selects which ADC drives the S/PDIF mixer
0C	ADC Selector 0	3	Audio Selector	Selects and amplifies/attenuates the input to ADC_0
0D	ADC Selector 1	3	Audio Selector	Selects and amplifies/attenuates the input to ADC_1
10	Digital Beep	7	Beep Generator	Internal digital PCBeep signal
11	Port A (Headphone)	4	Pin Complex	Front panel headphone/microphone jack
12	Port D (Front L/R)	4	Pin Complex	Rear panel front/headphone jack
13	Mono Out	4	Pin Complex	Monaural output pin (internal speakers or telephony system)
14	Port B (Front Mic)	4	Pin Complex	Front panel microphone/headphone jack
15	Port C (Line In)	4	Pin Complex	Rear panel line-in jack
16	Port F (Surr Back)	4	Pin Complex	Rear panel surround-rear (5.1) jack
17	Port E (Rear Mic)	4	Pin Complex	Rear panel mic jack
18	CD In	4	Pin Complex	Analog CD input
19	Mixer Power Down	5	Power Widget	Powers down the analog mixer and associated amps
1A	Analog PCBeep	4	Pin Complex	External analog PCBeep signal input
1B	S/PDIF Out	4	Pin Complex	S/PDIF output pin
1D	S/PDIF Mixer	2	Audio Mixer	Mixes the selected ADC with the digital stream to drive S/PDIF out
1E	Mono Out Mixer	2	Audio Mixer	Selects which source drives the mono out signal
20	Analog Mixer	2	Audio Mixer	Mixes individually gainable analog inputs
21	Mixer Output Atten	3	Audio Selector	Attenuates the mixer output to drive the port mixers
22	Port A Mixer	2	Audio Mixer	Mixes the Port A Selected DAC and mixer output amps to drive Port A
23	V_{REF} Power Down	F	Vendor Defined	Powers down the internal and external V_{REF} circuitry
24	Port G (C/LFE)	4	Pin Complex	Rear panel C/LFE jack
25	Port H (Surr Side)	4	Pin Complex	Rear panel surround-side (7.1) jack
26	Port E Mixer	2	Audio Mixer	Mixes DAC_2 and mixer output amps to drive Port E
27	Port G Mixer	2	Audio Mixer	Mixes DAC_2 and mixer output amps to drive Port G
28	Port H Mixer	2	Audio Mixer	Mixes DAC_0 and mixer output amps to drive Port H
29	Port D Mixer	2	Audio Mixer	Mixes DAC_1 and mixer output amps to drive Port D
2A	Port F Mixer	2	Audio Mixer	Mixes DAC_3 and mixer output amps to drive Port F
2B	Port B Mixer	2	Audio Mixer	Mixes the Port B selected DAC and mixer output amps to drive Port B
2C	Port C Mixer	2	Audio Mixer	Mixes the Port C selected DAC and mixer output amps to drive Port C
2D	Stereo Mix Down	2	Audio Mixer	Mixes the stereo L/R channels to drive mono output
2F	BIAS Power Down	F	Vendor Defined	Powers down the internal MIC_BIAS_FILT and all MIC_BIAS Pins
30	Port B Out Selector	3	Audio Selector	Selects the Port B DAC (0, 1)
31	Port C Out Selector	3	Audio Selector	Selects the Port C DAC (0, 3)
37	Port A Out Selector	3	Audio Selector	Selects the Port A DAC (0, 1)
38	Port A Boost	3	Audio Selector	Microphone boost amp for Port A
39	Port B Boost	3	Audio Selector	Microphone boost amp for Port B
3A	Port C Boost	3	Audio Selector	Microphone boost amp for Port C
3C	Port E Boost	3	Audio Selector	Microphone boost amp for Port E

HD AUDIO PARAMETERS

Table 6. Root and Function Node Parameters

Node ID	Name	Vendor ID 00	01	Revision ID 02[1]	03	Sub Node Count 04	Func. Group Type 05	Audio F.G. Caps 08	GPIO Caps 11
00	ROOT	11D41987		00100200		00010001			
01	FUNCTION					0002003B	00000001	00010C0C	40000002

[1] Subject to change with silicon stepping.

Table 7. SubSystem ID[1]

SubSystem ID			31:16	15:8	7:0
Node ID	Name	Value	SSID	SKU	Asm ID
01	FUNCTION	BFD40000	BFD7	00	00

[1] The default SSID is overwritten by platform BIOS after power-on. It is preserved across HD Audio link reset and verb reset.

WIDGET PARAMETERS

Table 8. Widget Parameters

Node ID	Widget Capabilities 09	PCM Size, Rate 0A	Stream Formats 0B	Pin Capabilities 0C	Input Amp Capabilities 0D	ConnList Length 0E	Power States 0F	Processing Capabilities 10	Output Amp Capabilities 12	Volume Knob Capabilities 13
01	00000480	000E01FF	00000001		80000000		00000009		00052727	
02	00030311	000E01E0	00000005			00000001				
03	00000405	000E01FF	00000001			00000000	00000009		00052727	
04	00000405	000E01FF	00000001			00000000	00000009		00052727	
05	00000405	000E01FF	00000001			00000000	00000009		00052727	
06	00000405	000E01FF	00000001			00000000	00000009		00052727	
08	00100501	000E01FF	00000001			00000001	00000009			
09	00100501	000E01FF	00000001			00000001	00000009			
0B	00300301					00000002				
0C	0030010D					00000008			80053627	
0D	0030010D					00000008			80053627	
10	0070000C					00000000			800B0F0F	
11	0040018D			0000373F		00000001			80000000	
12	0040058D			0001003F		00000001	00000009		80000000	
13	0040050C			00010010		00000001	00000009		80051F1F	
14	0040018D			0000373F		00000001			80000000	
15	0040018D			00003737		00000001			80000000	
16	0040018D			00000017		00000001			80000000	
17	0040098D			00003737		00000001			80000000	
18	00400001			00000020		00000000				
19	00500500					00000002	00000009			
1A	00400000			00000020		00000000				
1B	0040030D			00000010		00000001			80052727	
1D	00200303				80000000	00000002				
1E	00200103				80000000	00000002				
20	0020010B				80051F17	00000008				
21	0030010D					00000001			80051F1F	
22	00200103				80000000	00000002				
23	00F00100					00000008				
24	0040098D			00000017		00000001			80000000	
25	0040018D			00000017		00000001			80000000	
26	00200103				80000000	00000002				
27	00200103				80000000	00000002				
28	00200103				80000000	00000002				
29	00200103				80000000	00000002				
2A	00200103				80000000	00000002				
2B	00200103				80000000	00000002				
2C	00200103				80000000	00000002				
2D	00200100					00000001				
2F	00F00100					00000004				
30	00300101					00000002				
31	00300101					00000002				
37	00300101					00000002				
38	0030010D					00000001			00270300	
39	0030010D					00000001			00270300	
3A	0030010D					00000001			00270300	
3C	0030010D					00000001			00270300	

CONNECTION LIST

Table 9. Connection List

	Connections		0	1		2		3		4		5		6		7	
Node ID	[0–3]	[4–7]	NID	I	NID	I	NID	I	NID	I	NID	I	NID	I	NID	I	NID
02	0000001D		1D														
03																	
04																	
05																	
06																	
08	0000000C		0C														
09	0000000D		0D														
0B	00000908		08		09												
0C	18BC3938	20123B3B	38		39	1	3C		18		3B		3B		12		20
0D	18BC3938	20123B3B	38		39	1	3C		18		3B		3B		12		20
10																	
11	00000022		22														
12	00000029		29														
13	0000002D		2D														
14	0000002B		2B														
15	0000002C		2C														
16	0000002A		2A														
17	00000026		26														
18																	
19	00002120		20		21												
1A																	
1B	00000002		02														
1D	00000B01		01		0B												
1E	00002104		04		21												
20	12383A39	1A183B3C	39		3A		38		12		3C		3B		18		1A
21	00000020		20														
22	00002137		37		21												
23	A2209811	BC30AE24	11	1	18		20	1	22		24	1	2E		30	1	3C
24	00000027		27														
25	00000028		28														
26	00002105		05		21												
27	00002105		05		21												
28	00002103		03		21												
29	00002104		04		21												
2A	00002106		06		21												
2B	00002130		30		21												
2C	00002131		31		21												
2D	0000001E		1E														
2F	11171514		14		15		17		11								
30	00000403		03		04												
31	00000603		03		06												
37	00000403		03		04												
38	00000011		11														
39	00000014		14														
3A	00000015		15														
3C	00000017		17														

DEFAULT CONFIGURATION BYTES

In Table 10, default configuration values are set on codec power-up only. Default configuration values are not reset by link or soft reset to preserve modifications by BIOS control.

Table 10. Default Configuration Bytes

		31:30	29:28	27:24	23:20	19:16	15:12	8	7:4	3:0
			Location							
Name	Value	Connectivity	Chasis	Position	Def. Device	Conn Type	Color	JD OR	Def Assn	Sequence
Port A (Headphone)	0221401F	Jack	External	Front	HP Out	1/8″ Jack	Green	0	1	F
Port D (Line Out)	01014010	Jack	External	Rear	Line Out	1/8″ Jack	Green	0	1	0
Mono Out	991301F0	Fixed	Internal	Special 3	Speaker	ATAPI	Unknown	1	F	0
Port B (Front Mic)	02A190F0	Jack	External	Front	Mic In	1/8″ Jack	Pink	0	F	0
Port C (Line In)	01813021	Jack	External	Rear	Line In	1/8″ Jack	Blue	0	2	1
Port F (Surr Back)	01011012	Jack	External	Rear	Line Out	1/8″ Jack	Black	0	1	2
Port E (Rear Mic)	01A19020	Jack	External	Rear	Mic In	1/8″ Jack	Pink	0	2	0
CD IN	9933012E	Fixed	Internal	Special 3	CD	ATAPI	Unknown	1	2	E
Analog PCBeep	99F301F0	Fixed	Internal	Special 3	Other	ATAPI	Unknown	1	F	0
S/PDIF Out	014511F0	Jack	External	Rear	SPDIF Out	Optical	Black	1	F	0
Port G (C/LFE)	01016011	Jack	External	Rear	Line Out	1/8″ Jack	Orange	0	1	1
Port H (Surr Side)	01012014	Jack	External	Rear	Line Out	1/8″ Jack	Grey	0	1	4

OUTLINE DIMENSIONS

Dimensions are shown in millimeters.

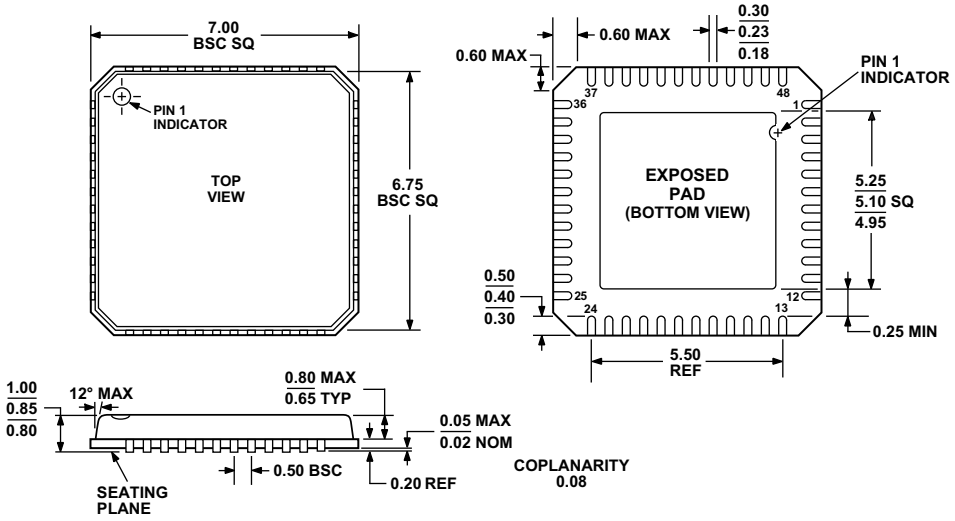

Figure 3. 48-Lead, Lead Frame Chip Scale Package [LFCSP_VQ]
7 mm × 7 mm Body, Very Thin Quad
(CP-48-1)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD1987JCPZ[1]	0°C to 70°C	48-Lead LFCSP_VQ	CP-48-1
AD1987JCPZ-RL[1]	0°C to 70°C	48-Lead LFCSP_VQ, 13" Tape and Reel	CP-48-1

[1] Z = RoHS Compliant Part.

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