

REALTEK

ALC658
ALC658-LF

SIX-CHANNEL AC'97 2.3 AUDIO CODEC

DATASHEET

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer’s general information on the Realtek ALC658 Audio CODEC chip.

Though every effort has been made to assure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
0.50	2003/01/27	Preliminary version.
0.60	2003/04/23	1.Pin 29 and 30 are designed as dedicated Front-Out to back panel. 2.Mono-Out is not supported. 3.Add jack detect pins JD3 and JD4 at pin 40 and pin 31.
1.0	2003/07/10	Official released version
1.10	2004/04/05	The LQFP-48 ‘e’ dimension is 0.0196 inch.
1.20	2005/03/14	Add section 12, Ordering Information, page 43. Add Lead (Pb)-free package & IC identification information on page 5.
1.3	2006/02/07	Update section 6.1.10, MX1A Record Select, page 13. Update section 12, Ordering Information, page 43. Add ESD data to Table 50, page 32. Add Power Supply Current and Power Down Current data to Table 63, page 39.

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1. General Description

The ALC658 has six channels of 20-Bit DAC, two pairs of stereo 18-Bit ADC, and an AC'97 2.3 compatible six channel audio CODEC designed for PC multimedia systems. The ALC658 incorporates proprietary converter technology to achieve 100dB sound quality. Not only to meet performance requirements on PC99/2001 systems, but also to make PC sound quality as good as consumer equipment.

The ALC658 CODEC provides three pairs of stereo outputs, with 6-Bit volume controls and multiple stereo and mono inputs, along with flexible mixing, and gain and mute functions to provide a complete integrated audio solution for PCs. The digital interface circuitry of the ALC658 CODEC operates from a 3.3V power supply for use in notebook and PC applications. The ALC658 integrates 50mW/20ohm headset audio amplifiers at Front-Out and AUX. Both are designed to be analog inputs and outputs automatically detected by hardware (Universal Audio Jack[®]).

To save BOM costs for motherboard makers, the ALC658 features a built-in high-accuracy 14.318M to 24.576MHz PLL, saving the cost of an extra 24.576MHz crystal. A PCBEEP generator is integrated and can be programmed by the BIOS to generate POST beeps without a buzzer. The ALC658 also supports S/PDIF input and output functions, which offers easy connection of PCs to consumer electronic products such as AC3 decoders/speakers, and mini disk devices.

The ALC658 supports host/soft audio from Intel ICHx chipsets, as well as audio controller based VIA/SIS/ALI/AMD/nVIDIA/ATI chipsets. Bundled Windows series (98/ME/NT/2000/XP) and Linux drivers, EAX/Direct Sound 3D/I3DL2/A3D compatible sound effect utilities (supporting Karaoke, 26-types of environment sound emulation, 10-band equalizer), HRTF 3D positional audio, and Sensaura[™] 3D (optional) providing an excellent entertainment package and game experience for PC users. The ALC658 also includes Realtek's impedance sensing techniques that allow device load on inputs and outputs to be detected.

2. Feature

- Meets performance requirements for audio on PC99/2001 systems
- Meets Microsoft WHQL/WLP 2.0 audio requirements
- Six Channels DA Converters with variable rate
- Two pairs of stereo AD Converters with variable rate
- **Compliant with AC'97 2.3 specifications**
 - Front-Out, Surround-Out, Cen/Lfe-Out, MIC-In and LINE-In Jack Sensing**
 - 14.318MHz to 24.576MHz PLL to save crystal**
 - 12.288MHz BITCLK input can be consumed**
 - Integrated PCBEEP generator to save buzzer**
 - Interrupt capability**
 - Page and Analog Plug & Play Registers**
- Three analog line-level stereo inputs with 5-bit volume control: LINE_IN, CD, AUX
- High quality differential CD input
- Two analog line-level mono input: PCBEEP, PHONE-IN
- Two software selectable MIC inputs
- A dedicated Front-MIC input for front panel applications (software selectable)
- **Dedicated Back-Front-Out pin.**
- +6/12/20/30dB boost preamplifier for MIC input
- LINE Input shared with surround out, MIC input shared with Center and LFE out (FlexJack®)
- 6-Bit volume control for Front-Out, Surround-Out and CEN/LFE-Out
- Both Front-out and AUX have integrated 50mW/20Ω amplifiers
- External Amplifier Power Down (EAPD)
- Power management and enhanced power saving features
- **Stereo MIC record for AEC/BF application**
- Supports **Power Off CD** function
- Adjustable VREFOUT control
- Supports double sampling rate (96KHz) of DVD audio playback
- Support 32K/44.1K/48K/96KHz of S/PDIF output
- Support 32K/44.1K/48KHz of S/PDIF input
- **2 Universal Audio Jacks (UAJ)® for front panel**
- **5 Jack Detect pins for automatic Jack sensing**
- Power support: Digital: 3.3V; Analog: 3.3V/5V
- Standard 48-Pin LQFP Package
- **EAX™ 1.0&2.0 compatible**
- **Direct Sound 3D™ compatible**
- **A3D™ compatible**
- **I3DL2 compatible**
- **HRTF 3D Positional Audio**
- **Sensaura™ 3D Enhancement** (optional)
- **10 Bands of Software Equalizer**
- **Voice Cancellation and Key Shifting in Karaoke mode**
- **AVRack® Media Player**
- **Configuration Panel to improve Experience of User**

3. Block Diagram

3.1. Analog Mixer

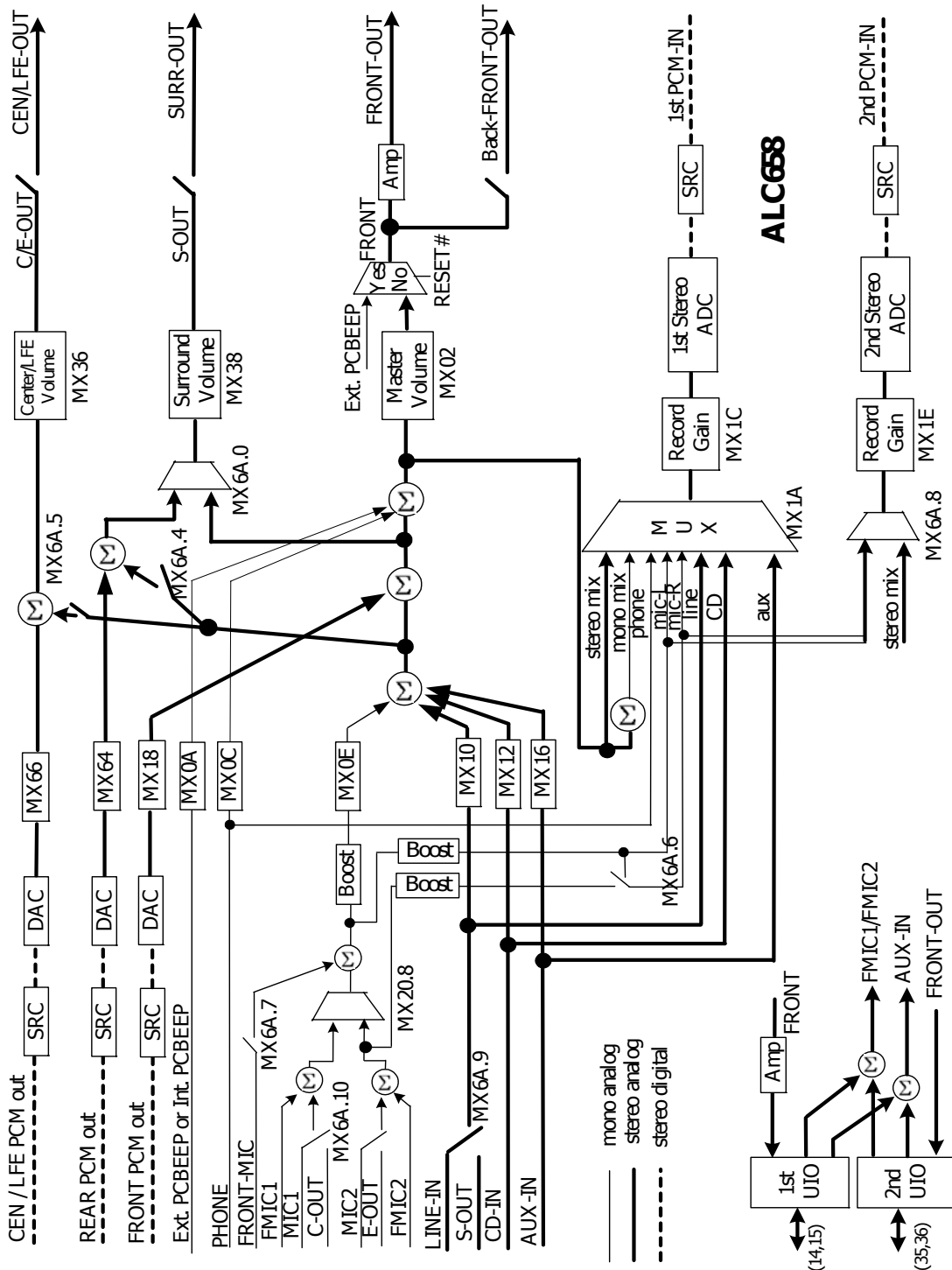


Figure 1. Analog Mixer

3.2. Digital Data Path

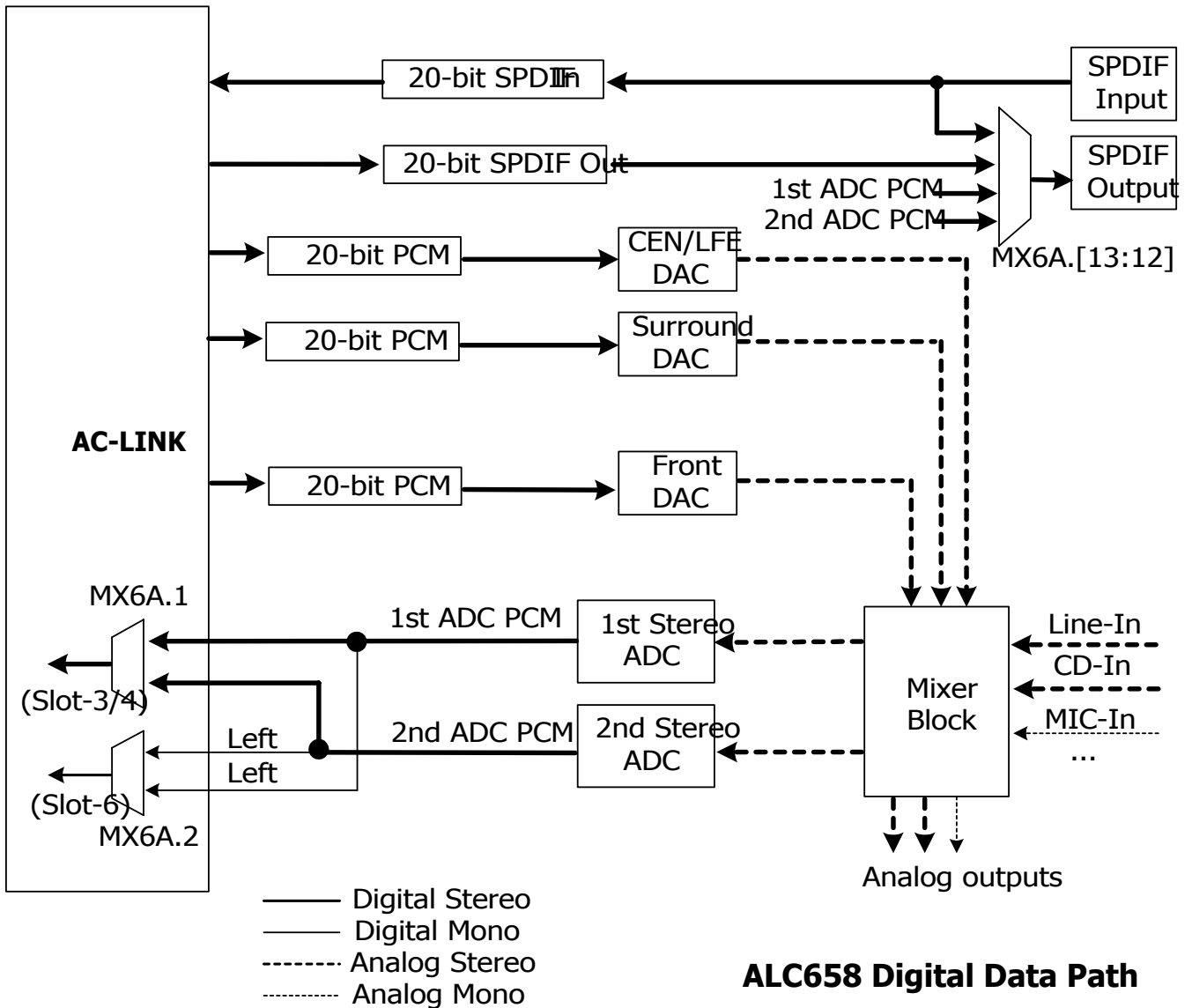


Figure 2. Digital Data Path

ALC658 Digital Data Path

4. Pin Assignments

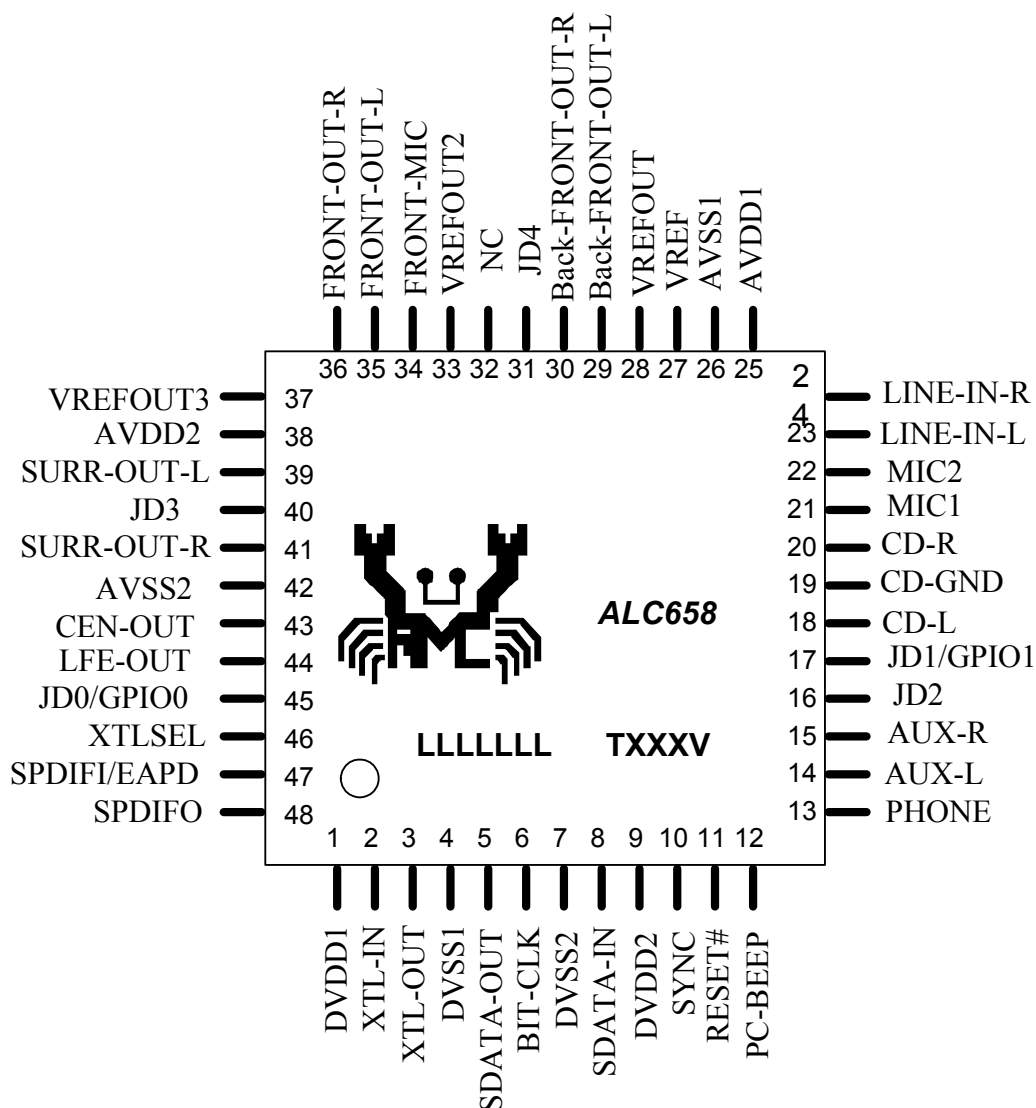


Figure 3. Pin Assignments

4.1. Lead (Pb)-Free Package and Version Identification

Lead (Pb)-free package is indicated by an 'L' in the location marked 'T' in Figure 3. The version number is shown in the location marked 'V'.

5. Pin Description

5.1. Digital I/O Pins

Table 1. Digital I/O Pins

Name	Pin No	Type	Description	Characteristic Definition
XTL-IN	2	I	Crystal input pad (24.576Mhz)	Crystal input pad
XTL-OUT	3	O	Crystal output pad	Crystal output pad
SDATA-OUT	5	I	Serial TDM AC'97 output	CMOS input
BIT-CLK	6	IO	Bit clock output (12.288Mhz)	CMOS input/output, $V_t=0.35V_{dd}$, internally pulled low by a 100K resistor.
SDATA-IN	8	O	Serial TDM AC'97 input	CMOS output, internal pulled low by a 100K resistor.
SYNC	10	I	Sample Sync (48Khz)	CMOS input
RESET#	11	I	AC'97 master H/W reset	CMOS input
JD2	16	I	Jack Detect pin 2	Internally pulled high to AVDD by a 100K resistor
JD1/GPIO1	17	I / O	Jack Detect pin 1/General Purpose I/O 1	Internally pulled high to AVDD by a 100K resistor
JD0/GPIO0	45	I/O	Jack Detect 0/General Purpose I/O 0	Internally pulled high to AVDD by a 100K resistor
JD3	I	40	Jack Detect pin 3	Externally pulled high to AVDD by a 100K resistor
JD4	I	31	Jack Detect pin 4	Externally pulled high to AVDD by a 100K resistor
XTLSEL	46	I	Crystal Selection	Internally pulled high
S/PDIFI / EAPD	47	I/O	S/PDIF input/External Amplifier power down control	Digital input/output
S/PDIFO	48	O	S/PDIF output	Digital output
TOTAL: 15 Pins				

*XTLSEL=floating, bypass 14.318MHz to 24.576MHz digital PLL. The clock source is 24.576MHz crystal or external clock.
XTLSEL=pull low, select 14.318MHz to 24.576MHz digital PLL*

5.2. Analog I/O Pins

Table 2. Analog I/O Pins

Pin Name	Pin No	Type	Description	Characteristic Definition
PC-BEEP	12	I	PC speaker input	Analog input (1Vrms)
PHONE	13	I	Speaker phone input	Analog input (1Vrms)
AUX-L	14	IO	AUX Left channel (UAJ2)	Analog input/output
AUX-R	15	IO	AUX Right channel (UAJ2)	Analog input/output
CD-L	18	I	CD audio Left channel	Analog input (1Vrms)
CD-GND	19	I	CD audio analog GND	Analog input (1Vrms)
CD-R	20	I	CD audio Right channel	Analog input (1Vrms)
MIC1	21	I / O	First Mic in / CEN-OUT	Analog input (1Vrms)/Analog output (1Vrms)
MIC2	22	I / O	Secondary Mic in/CEN-OUT	Analog input (1Vrms)/Analog output (1Vrms)
LINE-L	23	I / O	Line-In Left channel/S-OUT-L	Analog input (1Vrms)/Analog output (1Vrms)
LINE-R	24	I / O	Line-In Right channel/S-OUT-R	Analog input (1Vrms)/Analog output (1Vrms)
Front-MIC	34	I	Dedicated MIC Input	Analog input (1Vrms) for front panel MIC input
FRONT-OUTL	35	O	Front-Out Left channel (UAJ1)	Analog output (1Vrms)
FRONT-OUTR	36	O	Front-Out Right channel (UAJ1)	Analog output (1Vrms)
S-OUT-L	39	O	Surround Out Left channel	Analog output (1Vrms)
S-OUT-R	41	O	Surround Out Right channel	Analog output (1Vrms)
CEN-OUT	43	O	Center Out channel	Analog output (1Vrms)

Pin Name	Pin No	Type	Description	Characteristic Definition
LFE-OUT	44	O	Low Frequency Effect Out channel	Analog output (1Vrms)
Back-Front-OUT-L	O	29	Dedicated Front Out left channel w/o amplifier	Analog output (1Vrms)
Back-Front-OUT-R	O	30	Dedicated Front Out right channel w/o amplifier	Analog output (1Vrms)
				TOTAL: 20 Pins

5.3. Filter/Reference Pins

Table 3. Filter/Reference Pins

Name	Pin No	Type	Description	Characteristic Definition
VREF	O	27	Reference voltage	Analog output. +10uf cap to AVSS
VREFOUT	O	28	Ref. voltage out with 5mA drive	Analog output (2.5V)
VREFOUT2	O	33	Secondary Reference Voltage	Analog output (2.5V/4.0V)
VREFOUT3	O	37	Third Reference Voltage	Analog output (2.5V/4.0V)
NC		32	Not connected	
				TOTAL: 5 Pins

5.4. Power/Ground Pins

Table 4. Power/Ground Pins

Name	Pin No	Type	Description	Characteristic Definition
AVDD1	25	I	Analog VDD (5.0V)	The minimum value is 3.0V The maximum value is 5.5V
AVDD2	38	I	Analog VDD (5.0V)	The minimum value is 3.0V The maximum value is 5.5V
AVSS1	26	I	Analog GND	
AVSS2	42	I	Analog GND	
DVDD1	1	I	Digital VDD (3.3V)	The minimum value is 3.0V (DVdd-0.3) The maximum value is 3.6V (DVdd+0.3)
DVDD2	9	I	Digital VDD (3.3V)	The minimum value is 3.0V (DVdd-0.3) The maximum value is 3.6V (DVdd+0.3)
DVSS1	4	I	Digital GND	
DVSS2	7	I	Digital GND	
				TOTAL: 8 Pins

6. Register Descriptions

6.1. Mixer Registers

Access to registers with an odd number will return a 0. Reading unimplemented registers will also return a 0.

Table 5. Mixer Registers

Reg. (hex)	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0180h
02h	Master Volume	Mute	X	ML5	ML4	ML3	ML2	ML1	ML0	X	X	ML5	MR4	MR3	MR2	MR1	MR0	8000h
0Ah	PC_BEEP Volume	Mute	X	X	F7	F6	F5	F4	F3	F2	F1	F0	PB3	PB2	PB1	PB0	X	8000h
0Ch	PHONE Volume	Mute	X	X	X	X	X	X	X	X	X	X	PH4	PH3	PH2	PH1	PH0	8008h
0Eh	MIC Volume	Mute	X	X	X	X	X	X	X	X	20dB	X	MI4	MI3	MI2	MI1	MI0	8008h
10h	Line-In Volume	Mute	X	X	NL4	NL3	NL2	NL1	NL0	X	X	X	NR4	NR3	NR2	NR1	NR0	8808h
12h	CD Volume	Mute	X	X	CL4	CL3	CL2	CL1	CL0	X	X	X	CR4	CR3	CR2	CR1	CR0	8808h
16h	Aux Volume	Mute	X	X	AL4	AL3	AL2	AL1	AL0	X	X	X	AR4	AR3	AR2	AR1	AR0	8808h
18h	PCM Out Volume	Mute	X	X	PL4	PL3	PL2	PL1	PL0	X	X	X	PR4	PR3	PR2	PR1	PR0	8808h
1Ah	Record Select	X	X	X	X	X	LRS2	LRS1	LRS0	X	X	X	X	X	RRS2	RRS1	RRS0	0000h
1Ch	Record Gain	Mute	X	X	X	LRG3	LRG2	LRG1	LRG0	X	X	X	X	RRG3	RRG2	RRG1	RRG0	8000h
20h	General Purpose	X	X	X	X	X	X	MIX	MS	LBK	X	X	X	X	X	X	X	0000h
24h	Audio Int. & Paging	I4	I3	I2	I1	I0	X	X	X	X	X	X	X	PG3	PG2	PG1	PG0	0000h
26h	Power Down Ctrl/Status	EAPD	X	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	000Fh
28h	Extended Audio ID	0	0	X	X	REV1	REV0	0	LDAC	SDAC	CDAC	X	X	X	SPDIF	DRA	VRA	09C7h
2Ah	Extended Audio Status	X	X	PRK	PRJ	PRI	SPCV	X	LDAC	SDAC	CDAC	SPSA1	SPSA0	X	SPDIF	DRA	VRA	05F0h
2Ch	PCM front Sample Rate	1	0	1	1	1	0	1	1	1	0	0	0	0	0	0	0	BB80h
2Eh	PCM Surr. Sample Rate	1	0	1	1	1	0	1	1	1	0	0	0	0	0	0	0	BB80h
30h	PCM LFE. Sample Rate	1	0	1	1	1	0	1	1	1	0	0	0	0	0	0	0	BB80h
32h	PCM Input Sample Rate	1	0	1	1	1	0	1	1	1	0	0	0	0	0	0	0	BB80h
36h	Center/LFE Volume	Mute	X	LFE5	LFE4	LFE3	LFE2	LFE1	LFE0	Mute	X	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0	8080h
38h	Surround Volume	Mute	X	LSR5	LSR4	LSR3	LSR2	LSR1	LSR0	Mute	X	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0	8080h
3Ah	S/PDIF Ctl	V	0	SPSR1	SPSR0	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COPY	AUDIO	PRO	2000h
64h	Surr. DAC Volume	Mute	X	X	LSD4	LSD3	LSD2	LSD1	LSD0	X	X	X	RSD4	RSD3	RSD2	RSD1	RSD0	0808h
66h	CEN/LFE DAC Volume	Mute	X	X	LD4	LD3	LD2	LD1	LD0	X	X	X	CD4	CD3	CD2	CD1	CD0	0808h
6Ah	Multi-channel Ctl	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h

Reg. (hex)	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
7Ah	Extension Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	60A2h
7Ch	Vendor ID1	0	1	0	0	0	0	0	1	0	1	0	0	1	1	0	0	414Ch
7Eh	Vendor ID2	0	1	0	0	0	1	1	1	1	0	0	0	0	0	0	0	4780h

X = Reserved bit

*: MX36 is the master volume control of CENTER/LFE output.

MX38 is the master volume control of surround output.

6.1.1. MX00 Reset

Default: 0180H

Writing any value to this register will start a register reset and cause all of the registers to revert to their default values.

Reading this register returns the ID code of the specific part.

Table 6. MX00 Reset

Bit	Type	Function
15:10	-	Reserved
9	R	Read as 0 (Does not support 20-bit ADC)
8	R	Read as 1 (Supports 18-bit ADC)
7	R	Read as 1 (Supports 20-bit DAC)
6	R	Read as 0 (Does not support 18-bit DAC)
5	R	Read as 0 (No Loudness support)
4	R	Read as 0 (No True Line Level output support)
3	R	Read as 0 (No simulated stereo for analog 3D block use)
2	R	Read as 0 (No Bass & Treble Control)
1	R	Read as 0 (No Modem Line support)
0	R	Read as 0 (No Dedicated Mic PCM input channel)

Note: Writing any data into this register will reset all mixer registers to their default value. The written data is ignored.

6.1.2. MX02 (Front) Master Volume

Default: 8000H

These registers control the volume level of Front-Out. Each step on the left and right channels corresponds to a 1.5dB increase/decrease in volume.

Table 7. MX02 (Front) Master Volume

Bit	Type	Function
15	R/W	Mute Control 0: Normal 1: Mute ($-\infty$ dB)
14	-	Reserved
13:8	R/W	Master Left Volume (ML[5:0]) in 1.5 dB steps
7:6	-	Reserved
5:0	R/W	Master Right Volume (MR[5:0]) in 1.5 dB steps

For MR/ML: 00h 0 dB attenuation
 3Fh 94.5 dB attenuation

6.1.3. MX0A PC BEEP Volume

Default: 0000H

This register controls the input volume for the PC beep signal. Each step in bits 4:1 corresponding to a 3dB increase/decrease in volume. 16 levels of volume are available, from 0000 to 1111.

The purpose of this register is to allow the PC Beep signals to pass through the ALC658, eliminating the need for an external system speaker/buzzer. The PC BEEP pin is directly routed (internally hardwired) to the Front-Out. If the PC speaker/buzzer is eliminated, it is recommended to connect the external speakers at all times so the POST codes can be heard during reset.

Table 8. MX0A PC BEEP Volume

Bit	Type	Function
15	R/W	Mute Control 0: Normal 1: Mute ($-\infty$ dB)
14:13		Reserved
12:5	R/W	Internal PCBEEP Frequency, F[7:0] The internal PCBEEP frequency is the result of dividing the 48KHz clock by 4 times the number specified in F[7:0]. The lowest tone is $48\text{KHz}/(255*4)=47\text{Hz}$. The highest tone is $48\text{KHz}/(1*4)=12\text{KHz}$. A value of 00h in F[7:0] disables internal PCBEEP generator and allows external PCBEEP input.
4:1	R/W	PC Beep Volume (PBV[3:0]) in 3 dB steps
0		Reserved

For PB 00h 0 dB attenuation
 0Fh 45 dB attenuation

6.1.4. MX0C PHONE Volume

Default: 8008H

Register 0CH controls the telephone input volume for software modem applications. Because software modem applications may not have a speaker, the CODEC can offer a speaker-out service. Each step in bits 4:0 corresponds to a 1.5dB increase/decrease in volume, allowing 32 levels of volume, from 00000 to 11111.

Table 9. MX0C PHONE Volume

Bit	Type	Function
15	R/W	Mute Control 0: Normal 1: Mute ($-\infty$ dB)
14:5	-	Reserved
4:0	R/W	Phone Volume (PV[4:0]) in 1.5 dB steps

For PV: 00h +12 dB Gain
 08h 0 dB attenuation
 1Fh -34.5dB Gain

6.1.5. MX0E MIC Volume

Default: 8008H

Register 0EH controls the microphone input volume. Each step in bits 4:0 corresponds to a 1.5dB increase/decrease in volume, allowing 32 levels of volume, from 00000 to 11111. Each step in bit 6 corresponds to a 20dB increase in volume.

Table 10. MX0E MIC Volume

Bit	Type	Function
15	R/W	Mute Control 0: Normal 1: Mute ($-\infty$ dB)
14:10	-	Reserved
9:8	R/W	Boost Gain Option (BGO) 00: 20 dB 01: 6 dB 10: 12 dB 11: 29.5 dB ($V=30*V_{mic-in}$)
7	-	Reserved
6	R/W	20 dB Boost Control 0: Normal 1: 20 dB boost
5	-	Reserved
4:0	R/W	Mic Volume (MV[4:0]) in 1.5 dB steps

For MV: 00h +12 dB Gain
 08h 0 dB attenuation
 1Fh -34.5dB Gain

6.1.6. MX10 LINE_IN Volume

Default: 8808H

Register 10H controls the LINE_IN input volume. Each step in bits 4:0 corresponds to a 1.5dB increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 corresponds to a 1.5dB increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Table 11. MX10 LINE_IN Volume

Bit	Type	Function
15	R/W	Mute Control 0: Normal 1: Mute ($-\infty$ dB)
14:13	-	Reserved
12:8	R/W	Line-In Left Volume (NL[4:0]) in 1.5 dB steps
7:5	-	Reserved
4:0	R/W	Line-In Right Volume (NR[4:0]) in 1.5 dB steps

For NL/NR: 00h +12 dB Gain
 08h 0 dB Gain
 1Fh -34.5dB Gain

6.1.7. MX12 CD Volume

Default: 8808H

Register 12H controls the CD input volume. Each step in bits 4:0 corresponds to a 1.5dB increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 corresponds to a 1.5dB increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Table 12. MX12 CD Volume

Bit	Type	Function
15	R/W	Mute Control 0: Normal 1: Mute ($-\infty$ dB)
14:13	-	Reserved
12:8	R/W	CD Left Volume (CL[4:0]) in 1.5dB steps
7:5	-	Reserved
4:0	R/W	CD Right Volume (CR[4:0]) in 1.5dB steps

For CL/CR: 00h +12 dB Gain
 08h 0 dB Gain
 1Fh -34.5dB Gain

6.1.8. MX16 AUX Volume

Default: 8808H

Register 16H controls the auxiliary input volume. Each step in bits 4:0 corresponds to a 1.5dB increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 corresponds to a 1.5dB increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Table 13. MX16 AUX Volume

Bit	Type	Function
15	R/W	Mute Control 0: Normal 1: Mute ($-\infty$ dB)
14:13	-	Reserved
12:8	R/W	AUX Left Volume (AL[4:0]) in 1.5 dB steps
7:5	-	Reserved
4:0	R/W	AUX Right Volume (AR[4:0]) in 1.5 dB steps

For AL/AR: 00h +12 dB Gain
 08h 0 dB Gain
 1Fh -34.5dB Gain

6.1.9. MX18 PCM_OUT Volume

Default: 8808H

Register 18H controls the PCM_OUT output volume of front DAC. Each step in bits 4:0 corresponds to a 1.5dB increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 corresponds to a 1.5dB increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Table 14. MX18 PCM_OUT Volume

Bit	Type	Function
15	R/W	Mute Control 0: Normal 1: Mute ($-\infty$ dB)
14:13	-	Reserved
12:8	R/W	PCM Left Volume (PL[4:0]) in 1.5 dB steps
7:5	-	Reserved
4:0	R/W	PCM Right Volume (PR[4:0]) in 1.5 dB steps

For PL/PR: 00h +12 dB Gain
 08h 0 dB Gain
 1Fh -34.5dB Gain

6.1.10. MX1A Record Select

Default: 0000H

Register 1AH controls the record input source. Each step in bits 2:0 selects a recording source for the right channel. Each step in bits 10:8 selects a recording source for the left channel.

Table 15. MX1A Record Select

Bit	Type	Function
15:11	-	Reserved
10:8	R/W	Left Record Source Select (LRS[2:0])
7:3	-	Reserved
2:0	R/W	Right Record Source Select (RRS[2:0])

For LRS:

0	MIC
1	CD LEFT
2	Muted
3	AUX LEFT
4	LINE LEFT
5	STEREO MIXER OUTPUT LEFT
6	MONO MIXER OUTPUT
7	PHONE

For RRS:

0	MIC
1	CD RIGHT
2	Muted
3	AUX RIGHT
4	LINE RIGHT
5	STEREO MIXER OUTPUT RIGHT
6	MONO MIXER OUTPUT
7	PHONE

6.1.11. MX1C Record Gain for 1st Stereo ADC

Default: 8000H

Register 1CH controls the record gain. Each step in bits 3:0 corresponds to a 1.5dB increase/decrease in gain for the right channel, allowing 16 levels of gain, from 0000 to 1111. Each step in bits 11:8 corresponds to a 1.5dB increase/decrease in gain for the left channel, allowing 16 levels of gain, from 0000 to 1111.

Table 16. MX1C Record Gain for 1st Stereo ADC

Bit	Type	Function
15	R/W	Mute Control 0: Normal 1: Mute ($-\infty$ dB)
14:12	-	Reserved
11:8	R/W	Left Record Gain Select (LRG[3:0]) in 1.5 dB steps
7:4	-	Reserved
3:0	R/W	Right Record Gain Select (RRG[3:0]) in 1.5 dB steps

For LRG/RRG: 0Fh +22.5 dB Gain
00h 0 dB (No Gain)

6.1.12. MX1E Record Gain for 2nd Stereo ADC

Default: 8000H

Register 1EH controls the record gain. Each step in bits 3:0 corresponds to a 1.5dB increase/decrease in gain for the right channel, allowing 16 levels of gain, from 0000 to 1111. Each step in bits 11:8 corresponds to a 1.5dB increase/decrease in gain for the left channel, allowing 16 levels of gain, from 0000 to 1111.

Table 17. MX1C Record Gain for 2nd Stereo ADC

Bit	Type	Function
15	R/W	Mute Control 0: Normal 1: Mute (-∞ dB)
14:12	-	Reserved
11:8	R/W	Left Record Gain Select (LMRG[3:0]) in 1.5 dB steps
7:4	-	Reserved
3:0	R/W	Right Record Gain Select (RMRG[3:0]) in 1.5 dB steps

For LRG/RRG: 0Fh +22.5 dB Gain
00h 0 dB (No Gain)

6.1.13. MX20 General Purpose Register

Default: 0000H

This register is used to control several functions. Bit 13 enables or disables 3D control. Bit 9 allows selection of mono output. Bit 8 controls the MIC selector. Bit 7 enables loopback of the AD output to the DA input without involving the AC-Link, allowing for full system performance measurements.

Table 18. MX20 General Purpose Register

Bit	Type	Function
15:12	-	Reserved. Read as 0
11:10	R	DRSS[1:0], Double Rate Slot Select 00: PCM(n+1) data is on Slots 10/11 01: PCM(n+1) data is on Slots 7/8 (Default) 10, 11: Reserved
9	-	Reserved. Read as 0
8	R/W	MIC Select. 0: MIC1 1: MIC2
7	R/W	AD to DA Loop-Back Control 0: Disable 1: Enable
6:0	-	Reserved

Note: Bit 7 enables ADC to front DAC loop-back.

6.1.14. MX24 Audio Interrupt and Paging

Default: 0000h

Table 19. MX24 Audio Interrupt and Paging

Bit	Type	Function
15		Interrupt Status, I4 0: Interrupt is clear. 1: Interrupt was generated Interrupt event and status are clear by writing a 1 to this bit. The status will change regardless of interrupt enable (I0).
14	R	Interrupt Cause, I3 Reserved. Read as 0
13	R	Interrupt Cause, I2 I2=0: Sense value in page ID-01h MX6A.[12:8] has not changed. 1: Sense cycle completed or new sense value in page ID-01h MX6A.[12:8] is available. This bit reflects the cause of the first interrupt event generated. Software should read it after interrupt status (I4) has been confirmed as interrupting. I2 will be zero when I4 is cleared.
12	R/W	Sense Cycle, I1 0: Sense cycle not in progress 1: Sense cycle start Writing a '1' to this bit causes a sense cycle start. If a sense cycle is in progress, writing a '0' to this bit will abort the sense cycle. Whether the data in the sense result register (page ID-01h MX6A) is valid or not is determined by the IV bit in MX6A, Page ID-1h.
11	R/W	Interrupt Enable, I0 0: Interrupt is masked, interrupt status (I4) will not be shown in bit 0 of Slot 12 in SDATA-IN. 1: Interrupt is un-masked, interrupt status (I4) will be shown in bit 0 of Slot 12 in SDATA-IN. This bit controls the interrupt of the sense cycle.
10:4	NA	Reserved. Read as 0
3:0	R/W	Page Selector, PG[3:0] 0000b: Vendor Specific 0001b: Page ID 01 (AC'97 2.3 Discovery Descriptor Definition) Others: Reserved. This register is used to select a descriptor of 16 word pages between registers MX60 and MX6F. A value of 0 is used to select vendor specific space to maintain compatibility with the AC'97 2.2 vendor specific register. When PG[3:0] is not 0000b or 0001b, the ALC658 will return zero data for the ACLINK mixer read command.

6.1.15. MX26 Power Down Control/Status

Default: 0000H

This read/write register is used to program power-down states and monitor subsystem readiness. The lower half of this register is read-only; a '1' indicating that the subsection is 'ready'. Ready is defined as the subsection's ability to perform in its nominal state. When the AC-Link 'CODEC Ready' indicator bit (SDATA_IN slot 0, bit 15) is 1, it indicates that the AC-Link and AC'97 control and status registers are in a fully operational state. The AC'97 controller must further probe this power down control/status register to determine exactly which subsections, if any are ready.

Table 20. MX26 Power Down Control/Status

Bit	Type	Function
15	R/W	PR7 External Amplifier Power Down (EAPD) 0: EAPD output low (enable external amplifier) 1: EAPD output high (shut down external amplifier)
14	-	Reserved
13	R/W	PR5 0: Normal 1: Disable internal clock usage (BCLK remains output for modem CODEC)
12	R/W	PR4 0: Normal 1: Power down AC-Link
11	R/W	PR3 0: Normal 1: Power down Mixer (Vref off)
10	R/W	PR2 0: Normal 1: Power down Mixer (Vref still on)
9	R/W	PR1 0: Normal 1: Power down PCM DAC (front DAC)
8	R/W	PR0 0: Normal 1: Power down PCM ADCs and input MUX
7:4	-	Reserved. Read as 0
3	R	Vref Status 1: Vref is up to normal level 0: Not yet
2	R	Analog Mixer Status 1: Ready 0: Not yet
1	R	DAC Status 1: Ready 0: Not yet
0	R	ADC Status 1: Ready 0: Not yet

Table 21. Power Down Mode Truth Table

	CDAC	SDAC	LDAC	ADC	DAC	Mixer	Verf	AC-LINK	Int-CLK	EAPD	Front-AMP	Aux-AMP
PR0=1				PD								
PR1=1					PD							
PR2=1						PD					PD	PD
PR3=1	PD	PD	PD	PD	PD	PD	PD				PD	PD
PR4=1	PD	PD	PD	PD	PD			PD				
PR5=1	PD	PD	PD	PD	PD				PD			
PR7=1										High		
PRI=1	PD											
PRJ=1		PD										
PRK=1			PD									

PD: Power Down

High: Output High

Blank: Irrelevant

SDAC= Surround DAC

LDAC= LFE DAC

CDAC= Center DAC

PRI: Center DAC power down control bit defined in MX2A.11

PRJ: Surround DAC power down control bit defined in MX2A.12

PRK: LFE DAC power down control bit defined in MX2A.13

6.1.16. MX28 Extended Audio ID

Default: 09C6H

The Extended Audio ID register is a read-only register used to communicate information to the digital controller.

Table 22. MX28 Extended Audio ID

Bit	Type	Function
15:14	R	ID[1:0]. Always read as 0 (Only primary ID is supported)
13:12	-	Reserved. Read as 0
11:10	R	REV [1:0]=10 to indicate that the ALC658 is AC'97 rev. 2.3 compliant
9	R	AMAP. Read as 0.
8	R	LDAC. Read as 1 (LFE DAC is supported, according to AC'97 rev. 2.3)
7	R	SDAC. Read as 1 (Surround DAC is supported, according to AC'97 rev. 2.3)
6	R	CDAC. Read as 1 (Center DAC is supported, according to AC'97 rev. 2.3)
5:3	-	Reserved. Read as 0
2	R	S/PDIF. Read as 1 (S/PDIF output is supported)
1	R	DRA. Read as 1 (Double Rate Audio is supported)
0	R	VRA. Read as 1 (Variable Rate Audio is supported)

6.1.17. MX2A Extended Audio Status and Control Register

Default: 05F0H

This register contains two active bits for power down and status of the surrounding DACs. Bits 1 & 2 are read/write bits which are used to enable or disable DRA and S/PDIF respectively. Bits 4 & 5 are read/write bits used to determine the AC-LINK slot assignment of the S/PDIF. Bits 6, 7, & 8 are read-only bits that tell the controller when the Center, Surround, and LFE DACs are ready to receive data. Bit 10 is a read-only bit that tells the controller if the S/PDIF configuration is valid. Bits 11, 12, and 13 are read/write bits which are used to power down the Center, Surround, and LFE DACs respectively.

Table 23. MX2A Extended Audio Status and Control Register

Bit	Type	Function
15	R/W	VCFG. Validity Configuration of S/PDIF Output Combined with MX3A.15 to decide validity control in S/PDIF output signal.
14	-	Reserved.
13	R/W	Power Down LFE DAC. (PRK) 0: Normal 1: Power down LFE DAC
12	R/W	Power Down Surround DAC. (PRJ) 0: Normal 1: Power down Surround DAC
11	R/W	Power Down Center DAC. (PRI) 0: Normal 1: Power down Center DAC
10	R	SPCV (S/PDIF Configuration Valid) 0: Current S/PDIF configuration {SPSA, SPSR, DAC/slot rate} is not valid 1: Current S/PDIF configuration {SPSA, SPSR, DAC/slot rate} is valid
9	-	Reserved
8	R	LFE DAC Status (LDAC). 0: Not yet 1: Ready
7	R	Surround DAC Status (SDAC). 0: Not yet 1: Ready
6	R	Center DAC Status (CDAC). 0: Not yet 1: Ready
5:4	R/W	SPSA[1:0], S/PDIF-Out Slot Assignment when DRS=0 00: S/PDIF-Out source is from AC-LINK slot3/4. 01: S/PDIF-Out source is from AC-LINK slot7/8. 10: S/PDIF-Out source is from AC-LINK slot6/9. 11: S/PDIF-Out source is from AC-LINK slot10/11. (Default) SPSA[1:0], S/PDIF-Out Slot Assignment when DRS=1(for 96K S/PDIF-Out) 01: S/PDIF-Out source is from AC-LINK slot3/4 + slot7/8.
3	-	Reserved
2	R/W	S/PDIF Enable. 1: Enable 0: Disable (Hi-Z)
1	R/W	DRA Enable. 1: Enable 0: Disable ‡
0	R/W	VRA Enable. 1: Enable 0: Disable

Note 1: SPCV is a read-only bit that indicates whether the current S/PDIF-Out configuration is supported or not. If the configuration is supported, SPCV is set as 1 by H/W. The driver can check this bit to determine the status of the S/PDIF transmitter system. SPCV is always operating, independent of the S/PDIF enable bit (MX2A.2). The S/PDIF output is active if MX2A.2 is set in spite of SPCV. Once S/PDIF output is enabled but SPCV is invalid (SPCV=0), channel status is still output, but the output data bits will be all zero. The condition to allow S/PDIF output is S/PDIF(MX2A.2)=1 & SPACV=1, otherwise S/PDIF output will be all zeros when MX2A.2=1 and SPACV=0 (invalid).

Note 2: Only front DACs support a 96KHz sample rate when DRA=1. MX2A.1 only selects a clock source for the front DACs. Software must mute surround DACs and CEN/LFE DACs.

6.1.18. MX2C PCM Front/Center Output Sample Rate

Table 24. MX2C PCM Front/Center Output Sample Rate

Bit	Type	Function
15:0	R/W	Output Sampling Rate FOSR[15:0]

The ALC658 supports the following sampling rates, as required in the PC99/PC2001 design guide.

Sampling Rate	FOSR[15:0]
8000	1F40h
11025	2B11h
12000	2EE0
16000	3E80h
22050	5622h
24000	5DC0
32000	7D00h
44100	AC44h
48000	BB80h

Note: If the value written is not supported, the closest value is returned.

When MX2A.0=0 (VRA is disabled), this register will return BB80h when read.

6.1.19. MX2E PCM Surround Output Sample Rate

Table 25. MX2E PCM Surround Output Sample Rate

Bit	Type	Function
15:0	R	This is a read-only register and keeps the same value as that written to MX2C

6.1.20. MX30 PCM LFE Output Sample Rate

Default: BB80H

Table 26. MX30 PCM LFE Output Sample Rate

Bit	Type	Function
15:0	R	This is a read-only register and keeps the same value as that written to MX2C

6.1.21. MX32 PCM Input (1st ADC) Sample Rate

Default: BB80H

Table 27. MX32 PCM Input (1st ADC) Sample Rate

Bit	Type	Function
15:0	R/W	Output Sampling Rate IISR[15:0]

The ALC658 supports the following sampling rates, as required in the PC99/PC2001 design guide.

Sampling Rate	FISR[15:0]
8000	1F40h
11025	2B11h
12000	2EE0
16000	3E80h
22050	5622h
24000	5DC0
32000	7D00h
44100	AC44h
48000	BB80h

Note: If the value written is not supported, the closest value is returned.

When MX2A.0=0 (VRA is disabled), this register will return BB80h when read.

6.1.22. MX34 PCM Input (2nd ADC) Sample Rate

Default: BB80H

Table 28. MX34 PCM Input (2nd ADC) Sample Rate

Bit	Type	Function
15:0	R/W	Output Sampling Rate MISR[15:0]

The ALC658 supports the following sampling rates, as required in the PC99/PC2001 design guide.

Sampling Rate	MISR[15:0]
8000	1F40h
11025	2B11h
12000	2EE0
16000	3E80h
22050	5622h
24000	5DC0
32000	7D00h
44100	AC44h
48000	BB80h

Note: If the value written is not supported, the closest value is returned.

When MX2A.0=0 (VRA is disabled), this register will return BB80h when read.

6.1.23. MX36 LFE/Center Master Volume

Default: 8080H

Table 29. MX36 LFE/Center Master Volume

Bit	Type	Function
15	R/W	LFE Mute Control 0: Normal 1: Mute ($-\infty$ dB)
14	-	Reserved
13:8	R/W	LFE Master Volume (LFE[5:0]) in 1.5 dB steps
7	R/W	Center Mute Control 0: Normal 1: Mute ($-\infty$ dB)
6	-	Reserved
5:0	R/W	Center Master Volume (CNT[5:0]) in 1.5 dB steps

For LFE/CEN: 00h 0 dB
3Fh 94.5dB attenuation

6.1.24. MX38 Surround Master Volume

Default: 8080H

Table 30. MX38 Surround Master Volume

Bit	Type	Function
15	R/W	Left Mute Control 0: Normal 1: Mute ($-\infty$ dB)
14	-	Reserved
13:8	R/W	Surround Master Left Volume (LSR[5:0]) in 1.5 dB steps
7	R/W	Right Mute Control 0: Normal 1: Mute ($-\infty$ dB)
6	-	Reserved
5:0	R/W	Surround Master Right Volume (RSR[5:0]) in 1.5 dB steps

For LSR/RSR: 00h 0 dB
3Fh 94.5dB attenuation

6.1.25. MX3A S/PDIF Output Channel Status and Control

Default: 2000H

Table 31. MX3A S/PDIF Output Channel Status and Control

Bit	Type	Function
15	R/W	Validity Control (control V bit in Sub-Frame) 0: The V bit (valid flag) in the sub-frame depends on whether or not the S/PDIF FIFO has under-run 1: The V bit in the sub-frame is always sent as 1 to indicate the data is invalid.
14	R/W	DRS (Double Rate S/PDIF) 0: 32K, 44.1K, 48K S/PDIF-Out 1: 96K S/PDIF-Out This bit only can be set when SPSR is 10b.
13:12	R/W	SPSR[1:0] (S/PDIF Out Sample Rate) 00: sample rate is 44.1KHz , Fs[0:3]=0000 01: Reserved 10: Sample rate is 48.0KHz when DRS=0, Fs[0:3]=0100 (default) Sample rate is 96.0KHz when DRS=1, Fs[0:3]=0101 11: Sample rate set to 32.0KHz , Fs[0:3]=1100
11	R/W	LEVEL (Generation Level)
10:4	R/W	CC [6:0] (Category Code)
3	R/W	PRE (Pre-emphasis) 0: None 1: Filter pre-emphasis is 50/15 μ sec
2	R/W	COPY (Copyright) 0: Asserted 1: Not asserted
1	R/W	/AUDIO (Non-Audio Data type) 0: PCM data 1: AC3 or other digital non-audio data
0	R	PRO (Professional or Consumer format) 0: Consumer format 1: Professional format The ALC658 only supports consumer channel status format. This bit is always 0

To ensure the control and status information was sent (starting at bit31) at the beginning of S/PDIF transmission, MX3A.[14:0] should only be written to when the S/PDIF transmitter is disabled (MX2A.2=0).

If validity control is set (MX3A.15=1), the data bits (bit8 ~ bit27) should be forced to 0 to get better compatibility with Minidisks.

Table 32. Consumer Channel Status Block (bit0~bit31)

0	1	2	3	4	5	6	7
PRO=0	/AUDIO	COPY	PRE	0	0	0	0
8	9	10	11	12	13	14	15
CC0	CC1	CC2	CC3	CC4	CC5	CC6	LEVEL
16	17	18	19	20	21	22	23
0	0	0	0	0	0	0	0
24	25	26	27	28	29	30	31
Fs0	Fs1	Fs2	Fs3	0	0	0	0

The 'V' bit in the sub-frame is determined by Validity control (MX3A.15) and VCFG (MX2A.15).

Table 33. Validity Control S/PDIF Output

Validity	VCFG	Operation
0	0	If S/PDIF FIFO is under-run, the 'V' bit in the sub-frame is set to indicate that the S/PDIF data is invalid.
0	1	If S/PDIF FIFO is under-run, the 'V' bit in the sub-frame is always 0, and pads the data with '0's.
1	0	The 'V' bit is always 1, and data bits (bit 8 ~ bit 27) should be forced to 0.
1	1	The 'V' bit in the sub-frame is always '0', and the S/PDIF output data should be forced to zero.

6.2. Vendor Defined Registers (Page ID-00h)

These registers are available to Realtek and Realtek customers for specialized functions.

6.2.1. MX60 S/PDIF Input Channel Status [15:0]

Default: 0000h

The data in MX60 are captured from the channel status [15:0] of the S/PDIF-IN signal.

Table 34. MX60 S/PDIF Input Channel Status [15:0]

Bit	Type	Function
15	R	LEVEL (Generation Level)
14:8	R	CC[6:0] (Category Code)
7:6	R	Mode[1:0]
5:3	R	PRE[2:0] (Pre-Emphasis)
2	R	COPY (Copyright) 0: Asserted 1: Not Asserted
1	R	/AUDIO (Non-Audio Data type) 0: PCM data 1: AC3 or other digital non-audio data
0	R	PRO (Professional or Consumer Format) 0: Consumer Format 1: Professional Format The ALC658 only supports consumer channel status format. This bit is always 0

6.2.2. MX62 S/PDIF Input Channel Status [29:15]

Default: 0000h

The data in MX62 are captured from the channel status [29:16] of the S/PDIF-IN signal.

Table 35. MX62 S/PDIF Input Channel Status [29:15]

Bit	Type	Function
15	R	‘V’ bit in sub-frame of S/PDIFI, S/PDIFI_V 0: Data X and Y are valid 1: At least one of data X and Y is invalid This bit is real-time updated, and it is meaning when S/PDIF-IN is locked
14	R	S/PDIF-IN Input Signal Locked by hardware, S/PDIFI_LOCK 0: Unlocked 1: Locked
13:12	R	Ca[1:0] (Clock Accuracy)
11:8	R	Fs[3:0]. (Sample Frequency in channel status) 0000: 44.1KHz 0010: 48 KHz 0011: 32 KHz Others: Reserved
7:4	R	Cn[3:0] (Channel Number)
3:0	R	Sn[3:0] (Source Number)

Note: Bits [13:0] are captured from the channel status [29:16] of S/PDIFI.

Table 36. Consumer Channel Status of S/PDIFI (bit0~bit31)

0	1	2	3	4	5	6	7
PRO	/AUDIO	COPY	PRE0	PRE1	PRE2	Mode0	Model
8	9	10	11	12	13	14	15
CC0	CC1	CC2	CC3	CC4	CC5	CC6	LEVEL
16	17	18	19	20	21	22	23
Sn0	Sn1	Sn2	Sn3	Cn0	Cn1	Cn2	Cn3
24	25	26	27	28	29	30	31
Fs0	Fs1	Fs2	Fs3	Ca0	Ca1	0	0

The data from S/PDIF input is forced to 0 once the S/PDIF input signal is unlocked. Software must check this ‘LOCK’ bit before dealing with S/PDIF input operations.

6.2.3. MX64 Surround DAC Volume

Default: 0808H

Table 37. MX64 Surround DAC Volume

Bit	Type	Function
15	R/W	Mute Control 0: Normal 1: Mute ($-\infty$ dB)
14:13	-	Reserved
12:8	R/W	Surround DAC Left Volume (SDL[4:0]) in 1.5 dB steps
7:5	-	Reserved
4:0	R/W	Surround DAC Right Volume (SDR[4:0]) in 1.5 dB steps

For SDL/SDR: 00h +12 dB Gain
08h 0 dB Gain
1Fh -34.5 dB Gain

The default value is 0808H (unmuted).

6.2.4. MX66 Center/LFE DAC Volume

Default: 0808H

Table 38. MX66 Center/LFE DAC Volume

Bit	Type	Function
15	R/W	Mute Control 0: Normal 1: Mute ($-\infty$ dB)
14:13	-	Reserved
12:8	R/W	LFE DAC Volume (LD[4:0]) in 1.5 dB steps
7:5	-	Reserved
4:0	R/W	Center DAC Volume (CD[4:0]) in 1.5 dB steps

For LD/CD: 00h +12 dB Gain
 08h 0 dB Gain
 1Fh -34.5 dB Gain

The default value is 0808H (unmuted).

6.2.5. MX6A Data Flow Control

Default: 0000h

This register is used to control various parts of the ALC658 multi-channel functions.

Table 39. MX6A Data Flow Control

Bit	Type	Function
15	R/W	S/PDIF-IN Enable 0: Disable (Default) 1: Enable
14	R/W	S/PDIF-IN Monitoring Control 0: Disable, S/PDIF-IN data is not added to PCM data sent to DAC. (Default) 1: Enable, S/PDIF-IN data will be added to PCM data to DAC.
13:12	R/W	S/PDIF-Out Source 00: S/PDIF-Out data is from ACLINK controller. (Default) 01: S/PDIF-Out data is from 1 st ADC. 10: S/PDIF-Out data is from 2 nd ADC. 11: Buffered S/PDIF-IN signal is passed through to S/PDIF-Out.
11	R/W	Recorded PCM Data to ACLINK (SDATA-IN Slot 3/4) 0: Recorded PCM data to host is from ADC 1: Recorded PCM data to host is from S/PDIF-IN
10	R/W	MIC1 & MIC2/CENTER & LFE Output Control 0: Pin-21 is MIC1, pin-22 is MIC2 (Default) 1: Pin-21 is CENTER-Out, pin-22 is LFE-Out.
9	R/W	Line-In/Surround Output Control 0: pin-23 and pin-24 are analog input (Line-In). (Default) 1: pin-23 and pin-24 are duplicated output of surround channel (Surround-Out)
8	R/W	2 nd Stereo ADC Record Select 0: Stereo mix. (Default) 1: Left channel is from MIC-L, right channel is from MIC-R
7	R/W	FRONT-MIC Control 0: Enable (Default) 1: Disable
6	R/W	MIC Record Source 0: Mono duplicated. (Default) 1: Stereo
5	R/W	Analog Input Pass to Center/LFE Control 0: off (Default) 1: on
4	R/W	Analog Input Pass to Surround Control 0: off (Default) 1: on
3	R/W	Ignore V bit in sub-frame of S/PDIF-IN

Bit	Type	Function
		0: Disable, S/PDIF-IN FIFO will keep the last valid data (Default) 1: Enable, S/PDIF-IN FIFO will catch the S/PDIF-In data in spite of the V bit
2	R/W	SDATA-IN Slot 6 Source 0: 2 nd stereo ADC Left Channel (Default) 1: 1 st stereo ADC Left Channel
1	R/W	SDATA-IN Slot 3/4 Source (when MX6A.11=0) 0: 1 st stereo ADC (Default) 1: 2 nd stereo ADC
0	R/W	Surround Output Source. 0: S-OUT is the real surround output. (default) 1: S-OUT is the duplicated output of LINE-OUT

6.3. Discovery Descriptor (Page ID-01h)

These registers are defined in AC'97 2.3 for sensing and analog plug and play functions.

6.3.1. MX62 PCI Sub System ID

Default: FFFFh

Table 40. MX62 PCI Sub System ID

Bit	Type	Function
15:0	R/W	PCI Sub System Vendor ID This register can be written once only after power on, and is not affected by AC97 cold reset. The system manufacture's BIOS can set its own sub-system ID. The default value FFFFh means this register is implemented and data is not set by the BIOS.

6.3.2. MX64 PCI Sub Vendor ID

Default: FFFFh

Table 41. MX64 PCI Sub Vendor ID

Bit	Type	Function
15:0	R/W	PCI Vendor ID This register can be written only once after power on, and is not affected by a AC97 cold reset. The system manufacture's BIOS can set its own sub-vendor ID. The default value FFFFh means this register is implemented and data is not set by the BIOS.

6.3.3. MX66 Sense Function Select

Default: 0000h

Table 42. MX66 Sense Function Select

Bit	Type	Function
15:5		Reserved
4:1	R/W	Function Code bits, FC[3:0] These bits specify the type of audio function described in page ID 01h MX66, MX68, and MX6A. 0h: FRONT-OUT (pin-35/36) 1h: SURR-OUT (pin-39/41) 2h: CEN/LFE-Out (pin-43/44). 5h: MIC1 In (pin-21) 6h: MIC2 In (pin-22) 7h: LINE In (pin-23/24) Others: Reserved
0	R/W	Tip or Ring Selection, T/R This bit sets which jack conductor the sense value is measured from. It is combined with FC[3:0]. 0: Tip (Left channel) 1: Ring (Right channel)

6.3.4. MX68 Sense Function Information

Default: 02F1h

Table 43. MX68 Sense Function Information

Bit	Type	Function
15:5	-	Reserved
4	R/W	Information Valid bit, IV 0: After a sense cycle is completed indicates that no information is provided on the sensing method 1: After a sense cycle is completed indicates that information is provided on the sensing method Clear this bit by writing "1", writing '0' to this bit has no effect.
3:1	NA	Reserved
0	R	Function Information Present, FIP When this bit is set to '0', indicates that the G[4:0], INV, DL[4:0] and ST[2:0] bits are <i>not</i> supported.

6.3.5. MX6A Sense Detail

Default: 0000h

Table 44. MX6A Sense Detail

Bit	Type	Function
15:13	-	Reserved
12:8	R	Sense bits, S[4:0] (Default value depends on sensed result after Cold Reset) For output devices: (FC[3:0]= 0h, 1h, or 2h) 02h: Not specified or unknown 05h: Powered speaker 06h: Earphone or passive speaker Other: Not supported For input devices: (FC[3:0]= 5h, 6h, or 7h) 12h: Not specified or unknown 13h: Mono Microphone 15h: Stereo Line-In Other: Not supported This field reports the type of output/input peripheral plugged into the jack after sensing.
7:0	R	Always read as 0.

6.4. Extension Registers

6.4.1. MX76 GPIO & Interrupt Control

Default: 0000h

Table 45. MX76 GPIO & Interrupt Control

Bit	Type	Function
15	R/W	JDx(GPIOx) Status Indication in SDATA_IN 0: The status of JD0(GPIO0)/JD1(GPIO1)/JD2 and its valid tag are <i>not</i> indicated in SDATA_IN. 1: The status of JD0(GPIO0)/JD1(GPIO1)/JD2 and its valid tag are indicated in SDATA_IN
14	R/W	S/PDIFI Valid Interrupt Enable 0: Disable 1: Enable
13	R/W	S/PDIFI Lock Interrupt Enable 0: Disable 1: Enable
12		Reserved
11	R/W	MIC Sense Interrupt Enable 0: Disable 1: Enable. When the sense status bit in MX74.15 is changed, this will trigger the MIC Sense interrupt in bit0 of SDATA_IN's slot-12.
10	R/W	LINE-IN Sense Interrupt Enable 0: Disable 1: Enable. When the sense status bit in MX74.14 is changed, this will trigger the MIC Sense interrupt in bit0 of SDATA_IN's slot-12.
9:7		Reserved
6	R/W	JD2 Interrupt Enable (when it is used as input) 0: Disable 1: Enable. A low to high transaction will trigger the GPIO interrupt in bit0 of SDATA_IN's slot-12.
5	R/W	JD1(GPIO1) interrupt Enable (when it is used as input) 0: Disable 1: Enable. A low to high transaction will trigger the GPIO interrupt in bit0 of SDATA_IN's slot-12.
4	R/W	JD0(GPIO0) interrupt Enable (when it is used as input) 0: Disable 1: Enable. A low to high transaction will trigger the GPIO interrupt in bit0 of SDATA_IN's slot-12.
3:2		Reserved
1	R/W	GPIO1 Primitiveness Control 0: Set JD1(GPIO1) as input pin 1: Set JD1(GPIO1) as output pin
0	R/W	GPIO0 Primitiveness Control 0: Set JD0(GPIO0) as input pin. 1: Set JD0(GPIO0) as output pin.

6.4.2. MX78 GPIO & Interrupt Status

Default: 0000h

Table 46. MX78 GPIO & Interrupt Status

Bit	Type	Function
15	R/W	Extension register Write Enable 0: Disable 1: Enable This bit enables the write function for MX68/6A/6C in page-2h.
14	R/W	S/PDINF-In Valid Interrupt Status (S/PDIFIN_VIS). 0: No S/PDIFI Valid Interrupt 1: S/PDIFI Valid Interrupt S/PDIFIN_VIS = (MX76.14==1) & (S/PDIFI_V valid is changed) & (Locked) Write 1 to clear this status bit and its interrupt.
13	R/W	S/PDINF-In Lock Interrupt Status (S/PDIFIN_LIS). 0: No S/PDIFI Lock Interrupt 1: S/PDIFI LOCK interrupt S/PDIFIN_LIS = (MX76.13==1) & (S/PDIFI lock state is changed) Write 1 to clear this status bit and its interrupt.
12		Reserved
11	R	JD4 Input Status 0: JD4 is driven low by external device 1: JD4 is driven high by external device
10	R	JD3 Input Status 0: JD3 is driven low by external device 1: JD3 is driven high by external device
9	R/W	JD1(GPIO1) Output Control 0: Drive GPIO1 low. 1: Drive GPIO1 high.
8	R/W	JD0(GPIO0) Output Control 0: Drive GPIO0 low. 1: Drive GPIO0 high.
7		Reserved
6	R/W	JD2 Interrupt Status (JD2_IS). (When it is used as input) 0: No JD2 Interrupt 1: JD2 Interrupt JD2_IS = (MX76.6==1) & (JD2 transition) Write 1 to clear this status bit.
5	R/W	JD1(GPIO1) Interrupt Status (GPIO1_IS). (When it is used as input) 0: No JD0(GPIO1) Interrupt 1: JD1(GPIO1) Interrupt GPIO1_IS = (MX76.1==0) & (MX76.5==1) & (GPIO1 transition) Write 1 to clear this status bit.
4	R/W	JD0(GPIO0) Interrupt Status (GPIO0_IS). (When it is used as input) 0: No JD0(GPIO0) Interrupt 1: JD0(GPIO0) Interrupt GPIO0_IS = (MX76.0==0) & (MX76.4==1) & (GPIO0 transition) Write 1 to clear this status bit.
3		Reserved

Bit	Type	Function
2	R	JD2 Input Status 0: JD2 is driven low by external device (input) 1: JD2 is driven high by external device (input)
1	R	JD1(GPIO1) Input Status 0: JD1(GPIO1) is driven low by external device (input) 1: JD1(GPIO1) is driven high by external device (input)
0	R	JD0(GPIO0) Input Status 0: JD0(GPIO0) is driven low by external device (input) 1: JD0(GPIO0) is driven high by external device (input)

6.4.3. MX7A Miscellaneous Control

Default: 60A2H

Table 47. MX7A Miscellaneous Control

Bit	Type	Function
15:11	-	Reserved
10	R/W	Pin-37 Function Selection (MONO-OUT or Vrefout3) 0: Vrefout3 (Default) 1: MONO-OUT
9	R/W	Vrefout Off Control 0: Vrefout is normal on (Default) 1: Vrefout is off (In High-Z)
8	R/W	Vrefout2 / Vrefout3 Level Control (Default=0) 0: 2.5V 1: 4.0V
7:6	-	Reserved
5	R/W	SO-OUT 1K Ω Control (SO-Control) 0: Pin 39 and 41 are off 1: Pin 39 and 41 are on (Default)
4	R/W	CEN/LFE-OUT 1K Ω Control (C/E-Control) 0: Pin 43 and 44 are off 1: Pin 43 and 44 are on (Default)
3	R/W	JD2 Control Surround-Out, Center-Out and LFE-Out 0: Disable (Default) 1: Enable, when (MX7A.3=1 & MX78.2=1), Surr-Out and CEN/LFE-Out are muted
2	R/W	JD1 Control Surround-Out, Center-Out and LFE-Out 0: Disable (Default) 1: Enable, when (MX7A.2=1 & MX78.1=1 & MX76.1=0), Surr-Out and CEN/LFE-Out are muted
1	R/W	Pin-47 Function Selection 0: S/PDIF-IN (Default) 1: EAPD
0	R/W	JD0 Control Surround-Out, Center-Out and LFE-Out 0: Disable (Default) 1: Enable, when (MX7A.0=1 & MX78.0=1 & MX76.0=0), Surr-Out and CEN/LFE-Out are muted

6.4.4. MX7C Vendor ID1

Default: 414CH

The two registers (MX7C Vendor ID1 and MX7E Vendor ID2) contain four 8-bit ID codes. The first three codes have been assigned by Microsoft for Plug and Play definitions. The fourth code is a Realtek assigned code identifying the ALC658. The MX7C Vendor ID1 register contains the value 414Ch, which is the first and second characters of the Microsoft ID code. The MX7C Vendor ID2 register contains the value 4780h, which is the third character of the Microsoft ID code.

Table 48. MX7C VENDOR ID1

Bit	Type	Function
15:0	R	Vendor ID- "AL"

6.4.5. MX7E Vendor ID2

Default: 4780H

Table 49. MX7E VENDOR ID2

Bit	Type	Function
15:8	R	Vendor ID- "G"
7:4	R	Chip ID- 1000b (ALC658)
3:0	R	Version number- 0000b

7. Electrical Characteristics

7.1. Absolute Maximum Ratings

Table 50. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supplies:					
Digital	DVDD	3.0	3.3	3.6	V
Analog	AVDD	3.0	5.0	5.5	V
Ambient Operating Temperature	Ta	0	-	+70	°C
Storage Temperature	Ts			+125	°C
ESD (Electrostatic Discharge)					
Susceptibility Voltage					
Pin 33 (Vrefout2)			3000V		
Pin 37 (Vrefout3)			3500V		
Other			4500V		

7.1.1. Threshold Hold Voltage

Dvdd= 3.3V±5%, T_{ambient}=25°C, with 50pF external load.

Table 51. Threshold Hold Voltage

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input voltage range	V _{in}	-0.30	-	Dvdd+0.30	V
Low level input voltage (SYNC, SDATA_OUT, RESET#)	V _{IL}	-	0.7	0.35Dvdd	V
Low level input voltage (XTAL_IN,BIT_CLK)	V _{IL}	-	1.0	0.35Dvdd	V
Low level input voltage (Other digital pins)	V _{IL}	-	1.2	0.35Dvdd	V
High level input voltage (SYNC, SDATA_OUT, RESET#)	V _{IH}	0.4DVdd	1.7	-	V
High level input voltage (XTAL_IN,BIT_CLK)	V _{IH}	0.4DVdd	2.2	-	V
High level input voltage (Other digital pins)	V _{IH}	0.4DVdd	1.7	-	V
High level output voltage	V _{OH}	0.9DVdd		-	V
Low level output voltage	V _{OL}	-	-	0.1DVdd	V
Input leakage current	-	-10	-	10	μA
Output leakage current (Hi-Z)	-	-10	-	10	μA
Output buffer drive current	-	-	5	-	mA
Internal pull up resistance	-	30k	50k	100k	Ω

7.1.2. Digital Filter Characteristics

Table 52. Digital Filter Characteristics

Filter	Symbol	Minimum	Typical	Maximum	Units
ADC Lowpass Filter	Passband	0	-	19.2	KHz
	Stopband	28.8			KHz
	Stopband Rejection		-76.0		dB
DAC Lowpass Filter	Passband	0	-	19.2	KHz
	Stopband	28.8			KHz
	Stopband Rejection		-78.5		dB
	Passband Frequency Response		+/- 0.20		dB

7.1.3. S/PDIF Output Characteristics

Dvdd= 3.3V, T_{ambient}=25°C, with 75Ω external load.

Table 53. S/PDIF output Characteristics

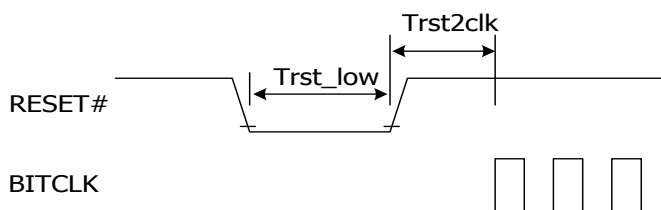
Parameter	Symbol	Minimum	Typical	Maximum	Units
High level output voltage	V _{OH}	3.0	3.3		V
Low level output voltage	V _{OL}	-	0	0.5	V

7.2. AC Timing Characteristics

7.2.1. Cold Reset

Table 54. Cold Reset

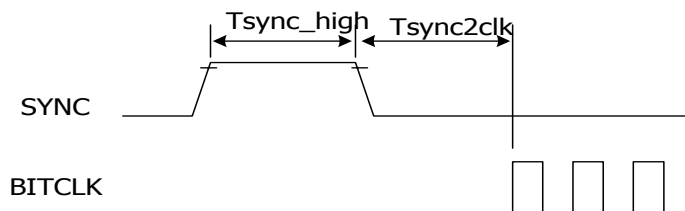
Parameter	Symbol	Minimum	Typical	Maximum	Units
RESET# active low pulse width	T _{rst_low}	1.0	-	-	μs
RESET# inactive to BIT_CLK Startup delay	T _{rst2clk}	162.8	-	-	ns


Figure 4. Cold Reset Timing Diagram

7.2.2. Warm Reset

Table 55. Warm Reset

Parameter	Symbol	Minimum	Typical	Maximum	Units
SYNC active high pulse width	$T_{\text{sync_high}}$	1.0	-	-	μs
SYNC inactive to BIT_CLK Startup delay	T_{sync2clk}	162.8	-	-	ns


Figure 5. Warm Reset Timing Diagram

7.2.3. AC-Link Clocks

Table 56. AC-Link Clocks

Parameter	Symbol	Minimum	Typical	Maximum	Units
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	$T_{\text{clk_period}}$	-	81.4	-	ns
BIT_CLK output jitter		-	-	750	ps
BIT_CLK high pulse width (note 2)	$T_{\text{clk_high}}$	36	40.7	45	ns
BIT_CLK low pulse width (note 2)	$T_{\text{clk_low}}$	36	40.7	45	ns
SYNC frequency		-	48.0	-	KHz
SYNC period	$T_{\text{sync_period}}$	-	20.8	-	μs
SYNC high pulse width	$T_{\text{sync_high}}$	-	1.3	-	μs
SYNC low pulse width	$T_{\text{sync_low}}$	-	19.5	-	μs

Note: Worse case duty cycle restricted to 45/55.

7.2.4. Data Output and Input Timing

Table 57. Data Output and Input Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
Output Valid Delay from rising edge of BIT_CLK	t_{co}	-	-	15	ns

Note 1: Timing is for SDATA and SYNC outputs with respect to BIT_CLK at the device driving the output

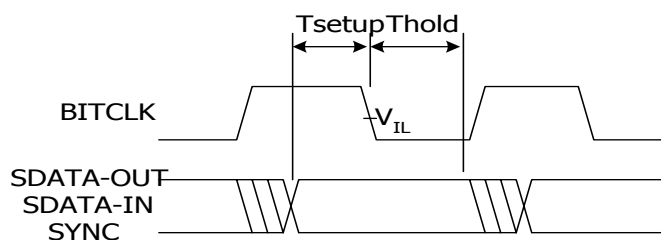
Note 2: 50pF external load

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Setup to falling edge of BIT_CLK	t_{setup}	10	-	-	ns
Input Hold from falling edge of BIT_CLK	t_{hold}	10	-	-	ns

Note: Timing is for SDATA and SYNC outputs with respect to BIT_CLK at the device driving the output

Parameter	Symbol	Minimum	Typical	Maximum	Units
BIT_CLK combined rise or fall plus flight time		-	-	7	ns
SDATA combined rise or fall plus flight time		-	-	7	ns

Note: Combined rise or fall plus flight times are provided for worst case scenario modeling purposes


Figure 6. Data Output and Input Timing Diagram

7.2.5. Signal Rise and Fall Timing

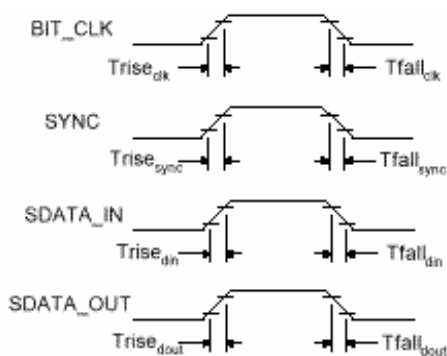
Table 58. Signal Rise and Fall Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
BIT_CLK rise time	$T_{rise_{clk}}$	-	-	6	ns
BIT_CLK fall time	$T_{fall_{clk}}$	-	-	6	ns
SYNC rise time	$T_{rise_{sync}}$	-	-	6	ns
SYNC fall time	$T_{fall_{sync}}$	-	-	6	ns
SDATA_IN rise time	$T_{rise_{din}}$	-	-	6	ns
SDATA_IN fall time	$T_{fall_{din}}$	-	-	6	ns
SDATA_OUT rise time	$T_{rise_{dout}}$	-	-	6	ns
SDATA_OUT fall time	$T_{fall_{dout}}$	-	-	6	ns

Note 1: 75pF external load (50 pF in AC'97 rev2.1)

Note 2: rise is from 10% to 90% of V_{dd} (V_{ol} to V_{oh})

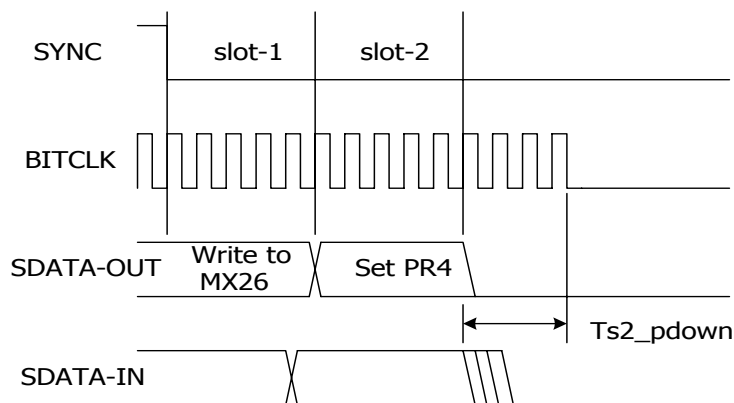
Note 3: fall is from 90% to 10% of V_{dd} (V_{oh} to V_{ol})


Figure 7. Signal Rise and Fall Timing Diagram

7.2.6. AC-Link Low Power Mode Timing

Table 59. AC-Link Low Power Mode Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
End of slot 2 to BIT_CLK, SDATA_IN low	T_{s2_pdown}	-	-	1.0	μs

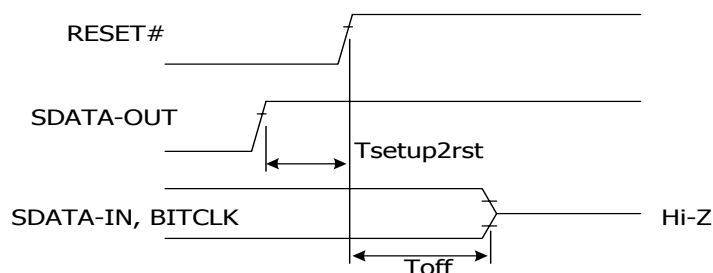

Figure 8. AC-Link Low Power Mode Timing Diagram

7.2.7. ATE Test Mode

To meet AC'97 rev. 2.3 specifications, EAPD, S/PDIFO, BIT_CLK and SDATA_IN should be floating in test mode.

Table 60. ATE Test Mode

Parameter	Symbol	Minimum	Typical	Maximum	Units
Setup to trailing edge of RESET# (also applies to SYNC)	$T_{\text{setup2rst}}$	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	T_{off}	-	-	25.0	ns


Figure 9. ATE Test Mode Timing Diagram

7.2.8. AC-Link IO Pin Capacitance and Loading

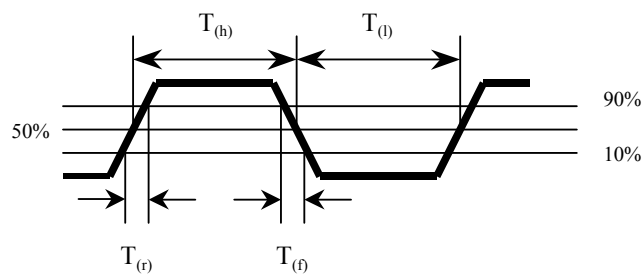
Table 61. AC-Link IO Pin Capacitance and Loading

Output Pin	1 CODEC	2 CODEC	3 CODEC	4 CODEC
BIT_CLK (must support ≥ 2 CODECs)	55pF	62.5pF	75pF	85pF
SDATA_IN	47.5pF	55pF	60pF	62.5pF

7.2.9. S/PDIF Output

Table 62. S/PDIF Output

S/PDIF_OUT	Minimum	Typical	Maximum	Units
Rise time/fall time	0		10	%
Duty cycle	45		55	%


Figure 6. S/PDIF Output

Rise time	$100 * T_{(r)} / (T_{(l)} + T_{(h)})\%$
Fall time	$100 * T_{(f)} / (T_{(l)} + T_{(h)})\%$
Duty cycle	$100 * T_{(h)} / (T_{(l)} + T_{(h)})\%$

8. Analog Performance Characteristics

Standard test conditions: $T_{\text{ambient}}=25^{\circ}\text{C}$, $D_{\text{vdd}}=3.3\text{V} \pm 5\%$, $A_{\text{vdd}}=5.0\text{V} \pm 5\%$
 1KHz input sine wave; Sampling frequency=48KHz; 0dB=1Vrms
 10K Ω /50pF load; Test bench Characterization BW: 10Hz~22KHz
 0dB attenuation; tone and 3D disabled

Table 63. Analog Performance Characteristics

Parameter	Minimum	Typical	Maximum	Units
Full scale input voltage: Line inputs (Mixers)	-	1.6	-	Vrms
Line inputs (A/D)	-	1.0	-	
Mic input (0 dB)	-	1.6	-	
Mic input (20 dB boost)	-	0.16	-	
Full scale output voltage				
FRONT-OUT/SURROUND-OUT	-	1.25	-	Vrms
CEN/LFE-OUT	-	1.25	-	Vrms
Analog to Analog S/N: CD to LINE-OUT	-	100	-	dB
Other to LINE-OUT	-	100	-	
Analog frequency response	10	-	22,000	Hz
S/N (A-weighted):	D/A	-	96	dB
	A/D	-	92	
Total Harmonic Distortion:	D/A	-	-90	dB
	A/D	-	-85	
D/A & A/D frequency response	20	-	19,200	Hz
Transition Band	19,200	-	28,800	Hz
Stop Band	28,800	-	∞	Hz
Stop Band Rejection	-75	-	-	dB
Out-of-Band Rejection	-	-65	-	dB
Group delay	-	-	1	ms
Power Supply Rejection	-	-65	-	dB
MIC Boost Gain	6		30	dB
Master Volume (FRONT/SURR/CEN/LFE): 64 step				
Step Size	-	1.5	-	dB
Attenuation Control Range	0	-	-94.5	dB
PC Beep Volume 16 steps:				
Step Size	-	3.0	-	dB
Attenuation Control Range	0	-	-45	dB
Analog Mixer Volume 32 steps:				
Step Size	-	1.5	-	dB
Gain Control Range	-34.5	-	+12	dB
Record Gain 16 steps:				
Step Size	-	1.5	-	dB
Gain Control Range	0	-	+22.5	dB
Input impedance (gain = 0dB, mixer = off)				
LINE-IN, CD-IN, AUX-IN, MIC1 / MIC2	-	64	-	K Ω
PCBEEP, PHONE	-	16	-	K Ω
Output Impedance				
FRONT-OUT /AUX with amplifier output	-	2	-	Ω
FRONT-OUT/ SURROUND-OUT/CEN/LFE-OUT	-	200	1000	Ω

Parameter	Minimum	Typical	Maximum	Units
Amplifier Maximum Output Power @20Ω load	-	-	50	mW
Power Supply Current				
VA=5.0V	-	60	-	mA
VA=3.3V	-	47	-	mA
VD=3.3V	-	28	-	mA
Power Down Current				
VA=5.0V / 3.3V	-	-	3/2.5	mA
VD=3.3V	-	-	1.1	mA
Vrefout/Vrefout2/Vrefout3	-	2.50	4.0	V
Vrefout Drive Current	-	5	-	mA

9. Design and Layout Guide

9.1. Clocking

The clock source is decided by XTLSEL latched from pin-46 after **power-on reset**. The clock source of different configurations is listed below:

Table 64. Clocking

Configuration	Operation & ID0		
	Pin-46 (XTLSEL)*	ID0	BIT-CLK
NC	0 (Primary)	Output 12.288MHz	Crystal or ext. 24.576MHz is attached at XTL-IN
Low**	0 (Primary)	Output 12.288MHz	Crystal or ext. 14.318MHz is attached at XTL-IN
NC	0 (Primary)	Input	12.288M input at BIT-CLK***

*Pin-46 is internally pulled high by a weak resistor.

**Low: Pulled low by a 0 ohm resistor. NC: Not Connected or pulled high.

***According to AC'97 ver 2.3, in Primary Mode, if a clock is present at BIT-CLK pin for at least 5 cycles before RESET# is de-asserted, the ALC658 is a consumer of BITCLK. The ALC658 uses external 12.288MHz BITCLK as its clock source.

9.2. AC-Link

When the ALC658 receives serial data from the AC97 controller, it samples SDATA_OUT on the falling edge of BIT_CLK. When the ALC658 sends serial data to the AC97 controller, it starts to drive SDATA_IN on the rising edge of BIT_CLK.

The ALC658 will return any uninstalled bits or registers with 0 for read operations. The ALC658 also stuffs the unimplemented slot or bit with 0's in SDATA_IN. Note that AC-LINK is MSB-justified.

Refer to "Audio CODEC '97 Component Specification Revision 2.3." for details.

Table 65. AC-Link

Slot#	0	1	2	3	4	5	6	7	8	9	10	11	12
SYNC	[Timing diagram showing SYNC signal across slots 0-12]												
SDATA-OUT	TAG	CMD	DATA	PCM L	PCM R		CEN	SURR L	SURR R	LFE	S/PDIF L	S/PDIF L	
SDATA-IN	TAG	ADD	DATA	PCM L	PCM R								

Default ALC658 Slot Arrangement – CODEC ID = 00 (the ALC658 supports primary mode only)

9.3. Reset

There are 3 types of reset operations: Cold, Warm, and Register.

Table 66. Reset

Reset Type	Trigger Condition	CODEC Response
Cold	Assert RESET# for a specified period	Reset all hardware logic and all registers to default values.
Register	Write register indexed 00h	Reset all registers to default values.
Warm	Driven SYNC high for specified period without BIT_CLK	Reactivates AC-LINK, no change to register values.

The AC97 controller should drive SYNC and SDATA_OUT low during the period of RESET# assertion to guarantee that the ALC658 has reset successfully.

9.4. CD Input

For noise cancellation reasons, it is important to pay attention to differential CD input. Below is an example of differential CD input.

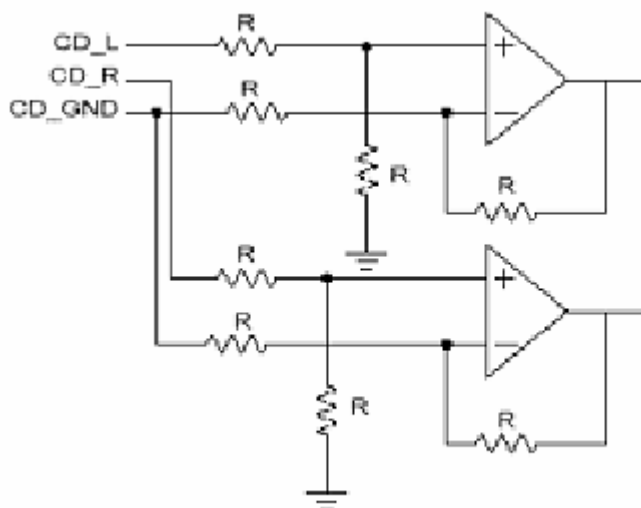


Figure 7. Example of Differential CD Input

9.5. Odd Addressed Register Access

The ALC658 will return '0000h' when odd-addressed and unimplemented registers are read.

9.6. Power Down Mode

For power saving reasons, it is important to pay special attention to the power down control register (index 26h), especially PR4 (power down AC-link).

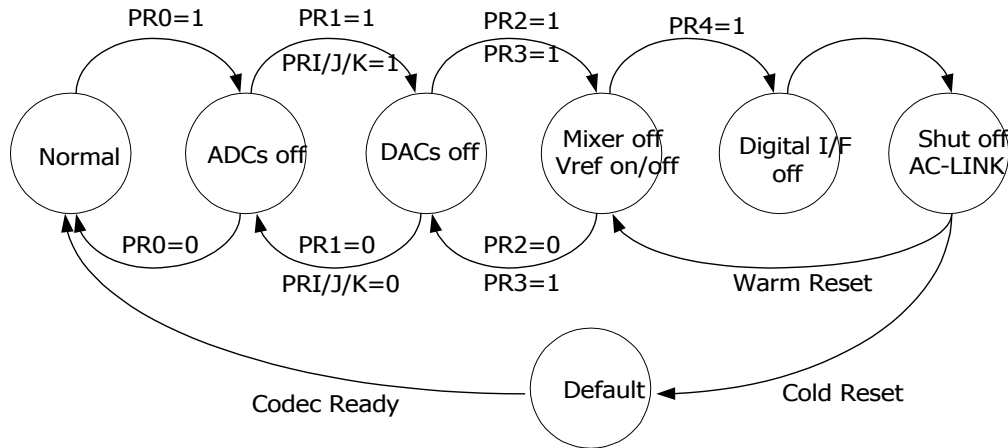


Figure 83. Power Down Control

9.7. Test Mode

To provide compatibility with AC'97 rev2.2, the ALC658 will float its digital output pins in both ATE and Vendor-Specific test modes. Refer to AC'97 rev 2.2 section 9.2 for a detailed description of the test modes.

9.7.1. ATE in Circuit Test Mode

SDATA_OUT is sampled high at the trailing edge of RESET#. In this mode, the ALC658 will drive BIT_CLK, SDATA_IN, EAPD, and S/PDIFO to high impedance.

9.7.2. Vendor Specific Test Mode

Vendor Specific Test mode is no longer supported.

9.8. POWER OFF CD Function

The 'POWER OFF CD' function describes a state after the system has been shut down (digital power is off) and a +5V analog power is supplied, the ALC658 will turn on the CD-IN op-amp and output amplifier. It is possible to design a system that can save op-amp circuitry and bypass CD output directly to the speaker.

The figure below indicates the system application circuitry that supports the 'POWER OFF CD' function. The operation mode is determined by +3.3VCC and +5VA. Analog power **without VAUX** is required for ALC20x series CODECS.

Table 67. Power OFF CD Function Circuitry

+3.3VCC	+5VA	+5Vstandby	Operation Mode
No (0)	No (0)	No (0)	Shut Down
No (0)	Yes (1)	-	Power Off CD
No (0)	-	Yes (1)	Power Off CD
Yes (1)	No (0)	No (0)	Digital on, Analog is off
Yes (1)	Yes (1)	-	Normal

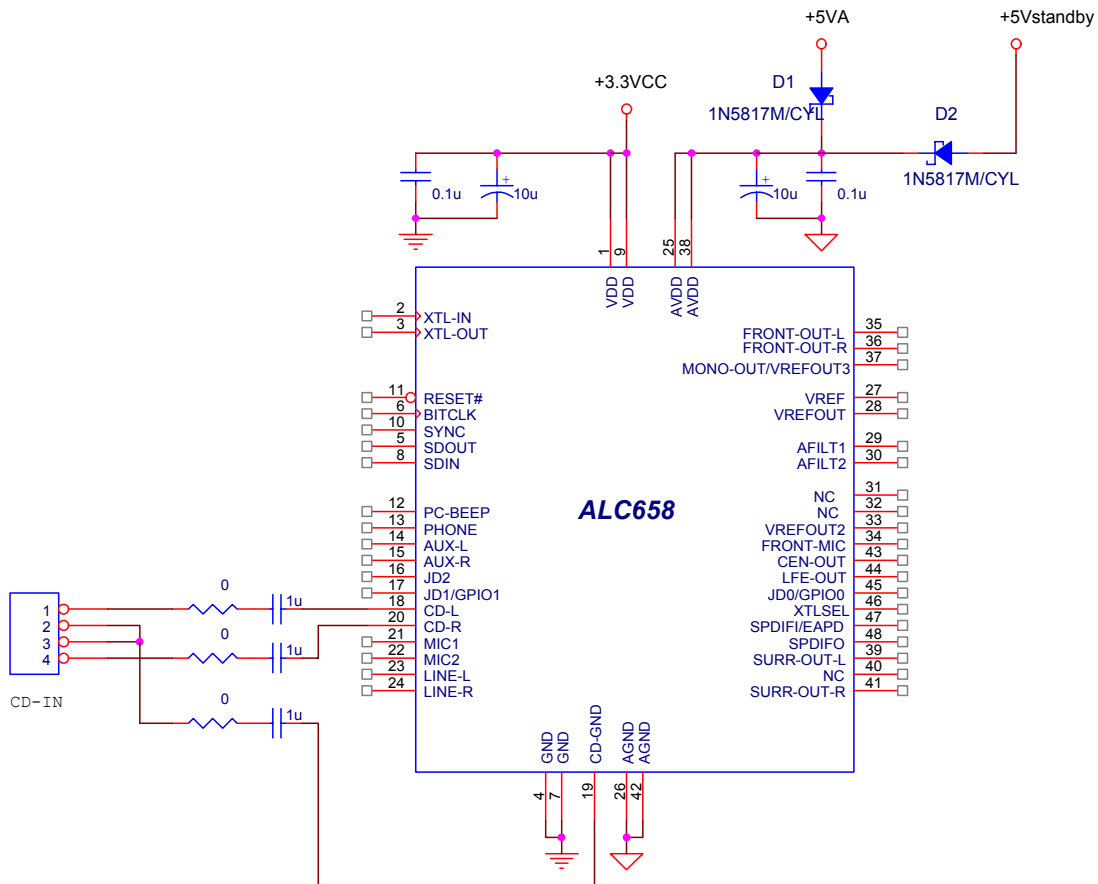
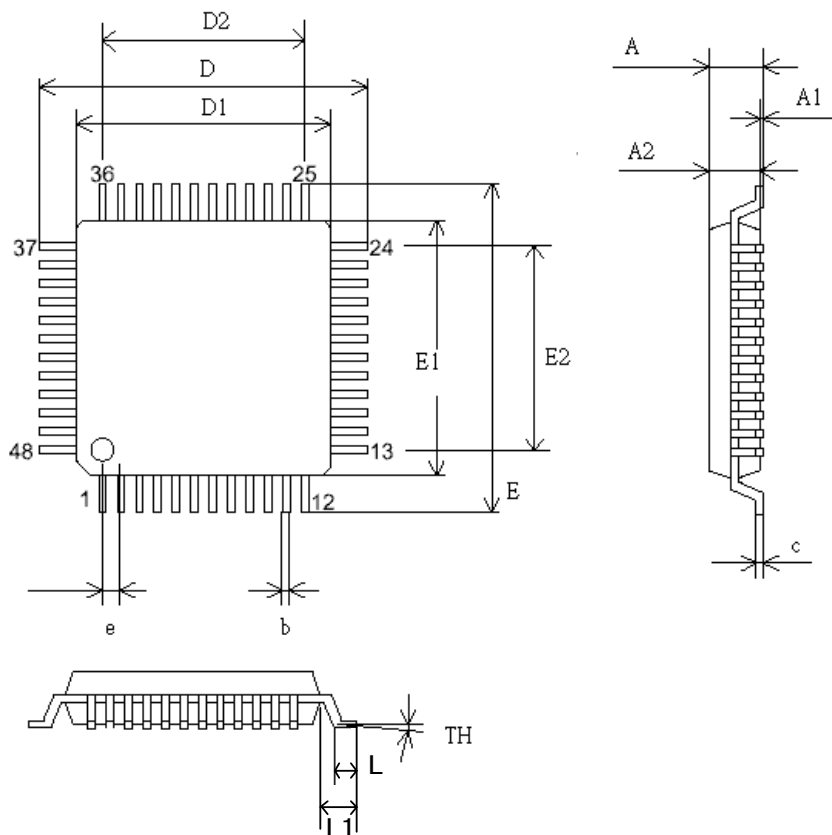


Figure 9. Power OFF CD Function Circuitry

10. Application Circuits

System designers are suggested to visit Realtek's web site to download the latest application circuits. To get the best compatibility in hardware design and software driver, any modifications of application circuits should be confirmed by Realtek.

11. Mechanical Dimensions



SYMBOL	MILLIMETER			INCH		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
C	0.09		0.20	0.004		0.008
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
D2	5.50			0.217		
E	9.00 BSC			0.354 BSC		
E1	7.00BSC			0.276 BSC		
E2	5.50			0.217		
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC			0.0196 BSC		
TH	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.0236	0.030
L1		1.00			0.0393	

TITLE: LQFP-48 (7.0x7.0x1.6mm)		
PACKAGE OUTLINE DRAWING, FOOTPRINT 2.0mm		
LEADFRAME MATERIAL		
APPROVE	DOC. NO.	
	VERSION	02
CHECK	DWG NO.	PKGC-065
	DATE	
REALTEK SEMICONDUCTOR CORP.		

12. Ordering Information

Table 68. Ordering Information

Part Number	Package	Status
ALC658	Standard product. LQFP-48	Production
ALC658-LF	ALC658 with Lead (Pb)-Free package	Production

Note 1: See page 5 for lead (Pb)-free package and version identification.

Note 2: Above parts are tested under AVDD = 5.0V. If customers have lower AVDD request, please contact Realtek sales representatives or agents.

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