



**RADEON X1000  
Memory Controller**

# Ring Bus Memory Controller



## Supports today's fastest graphics memory devices

- GDDR3, 48+ GB/sec

## 512-bit Ring Bus

- Simplifies layout and enables extreme memory clock scaling

## New Cache Design

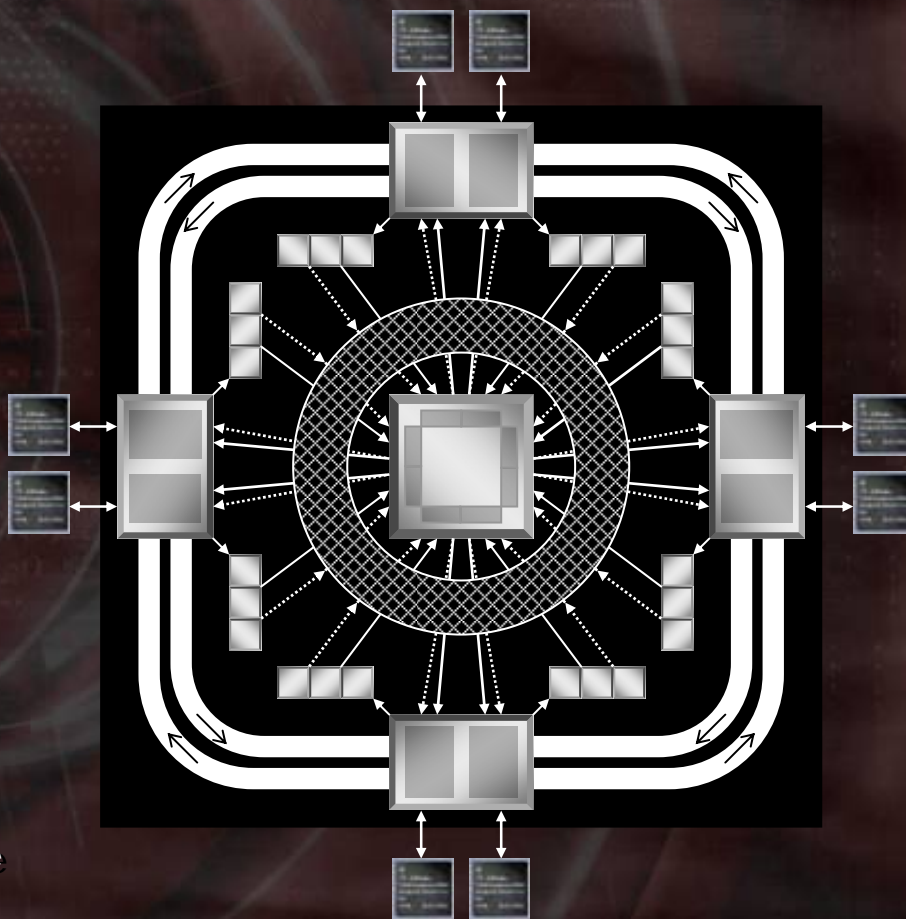
- Fully Associative for more optimal performance

## Improved Hyper Z

- Better compression and hidden surface removal

## Programmable Arbitration Logic

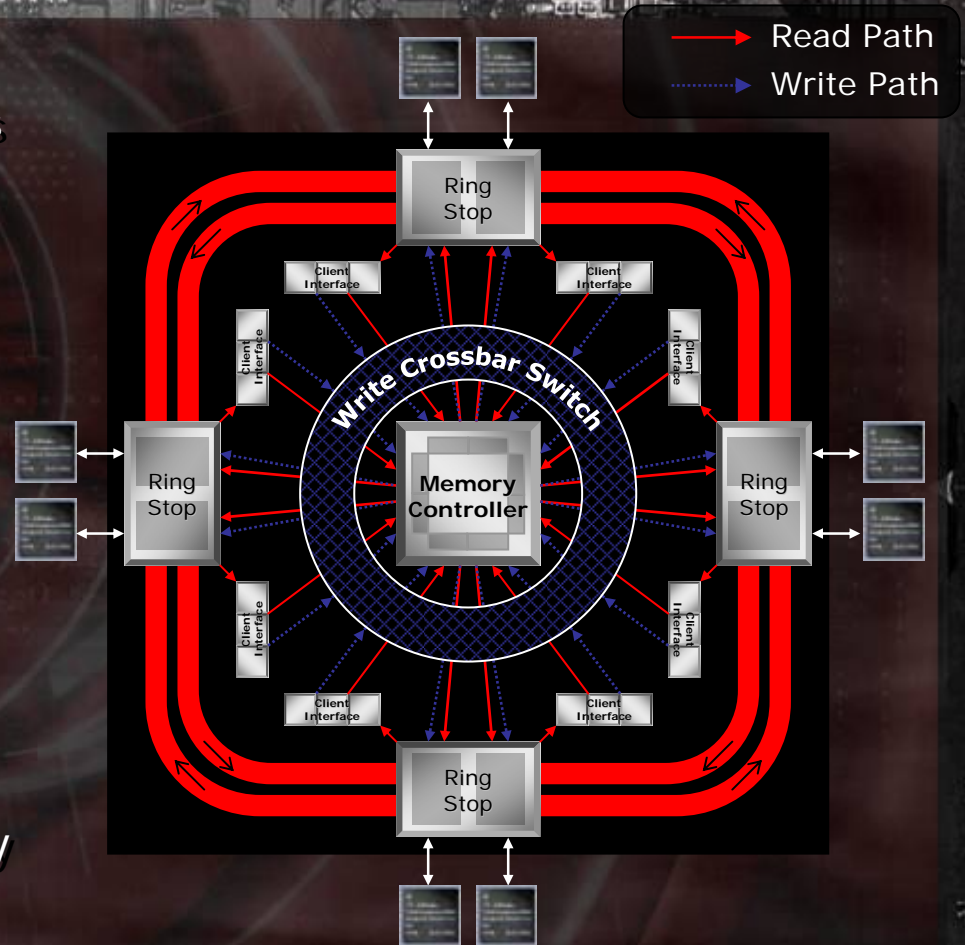
- Maximizes memory efficiency
- Can be upgraded via software



# Radeon X1800 Ring Bus



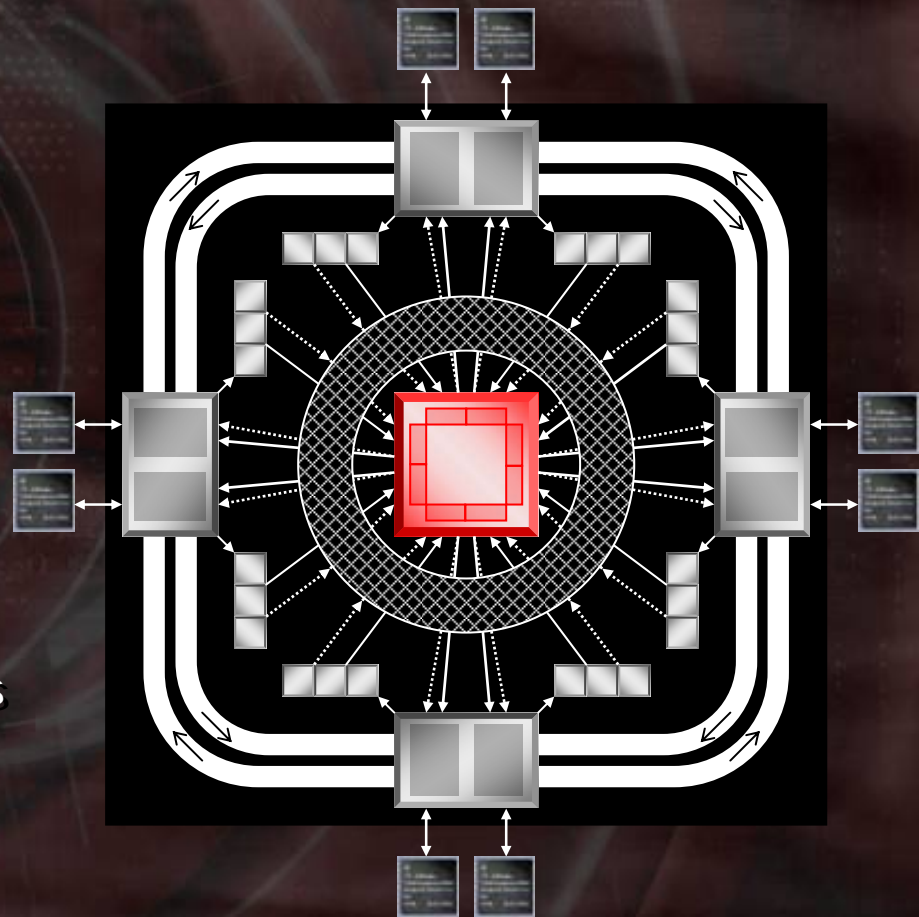
- Two internal 256-bit rings
  - Run in opposite directions to minimize latency
  - Return requested data to clients
  - Memory writes use crossbar switch
- Circle around the periphery of the chip
  - Reduces routing complexity
  - Permits higher clock speeds
- One ring stop per pair of memory channels
  - Linked directly to memory interface



# Programmable Arbitration Logic



- Prioritizes memory access requests
  - Predicts impact of each request on overall performance
- Uses feedback system to maximize memory and GPU efficiency
- Programmable parameters
  - Can be tuned via driver updates

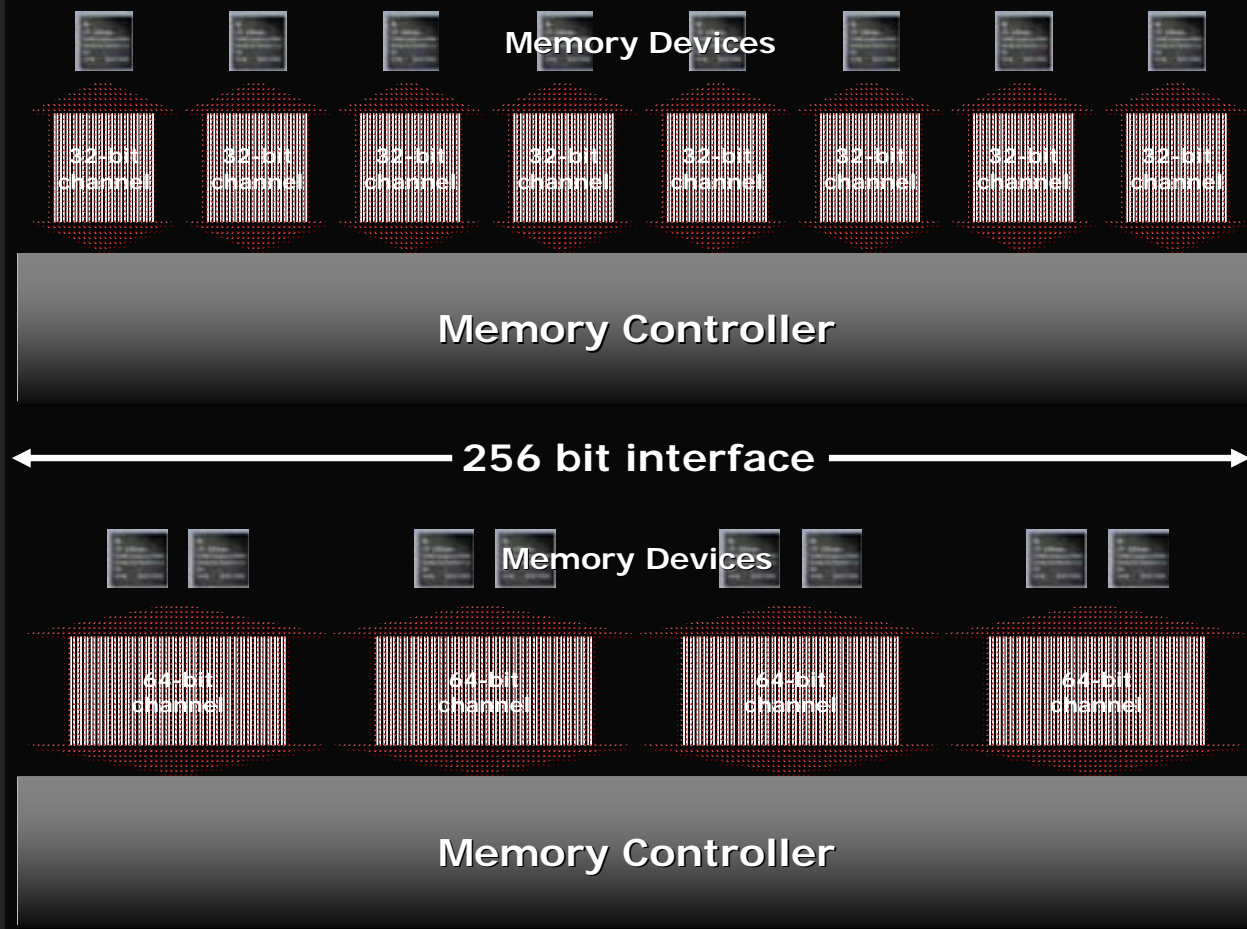


# Memory Channels



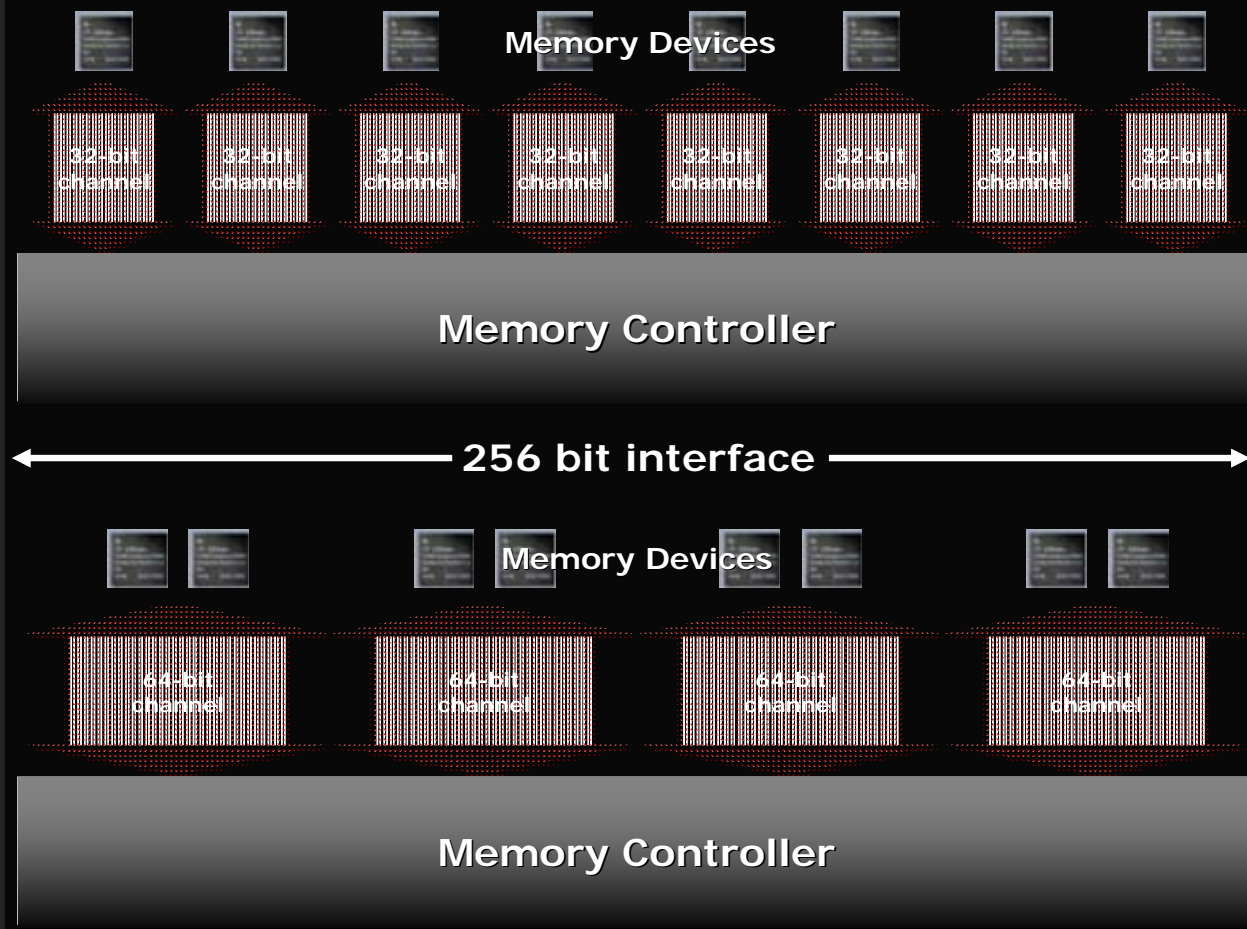
## Radeon X1800

3x32-bit channels



## Radeon X350

4x64-bit channels



# Cache Design



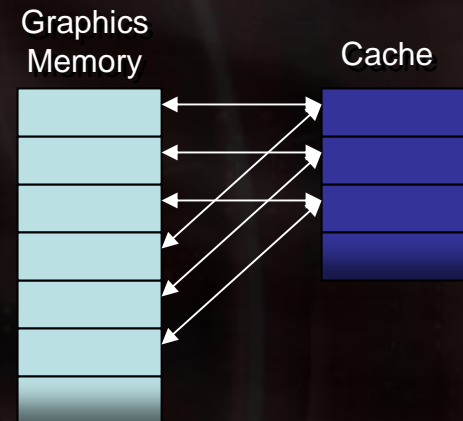
## Fully Associative Caches

- Cache lines can map to any location in external memory
- Earlier designs used Direct Mapped & N-Way Associative Caches
- Could only access limited blocks of external memory

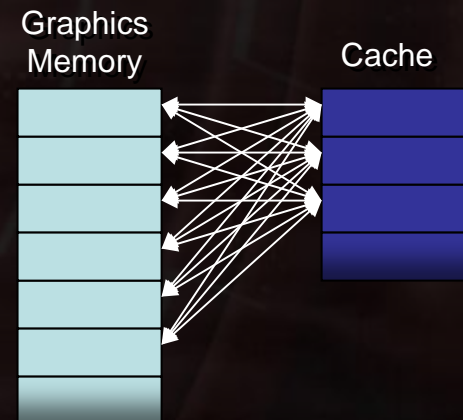
## Texture, Color, Z & Stencil caches are all now fully associative

- Reduces memory bandwidth requirements
- Minimizes cache contention stalls
- Optimized game performance
- Gains up to 25% clock for clock in fill/bandwidth bound cases

### Direct Mapped Cache



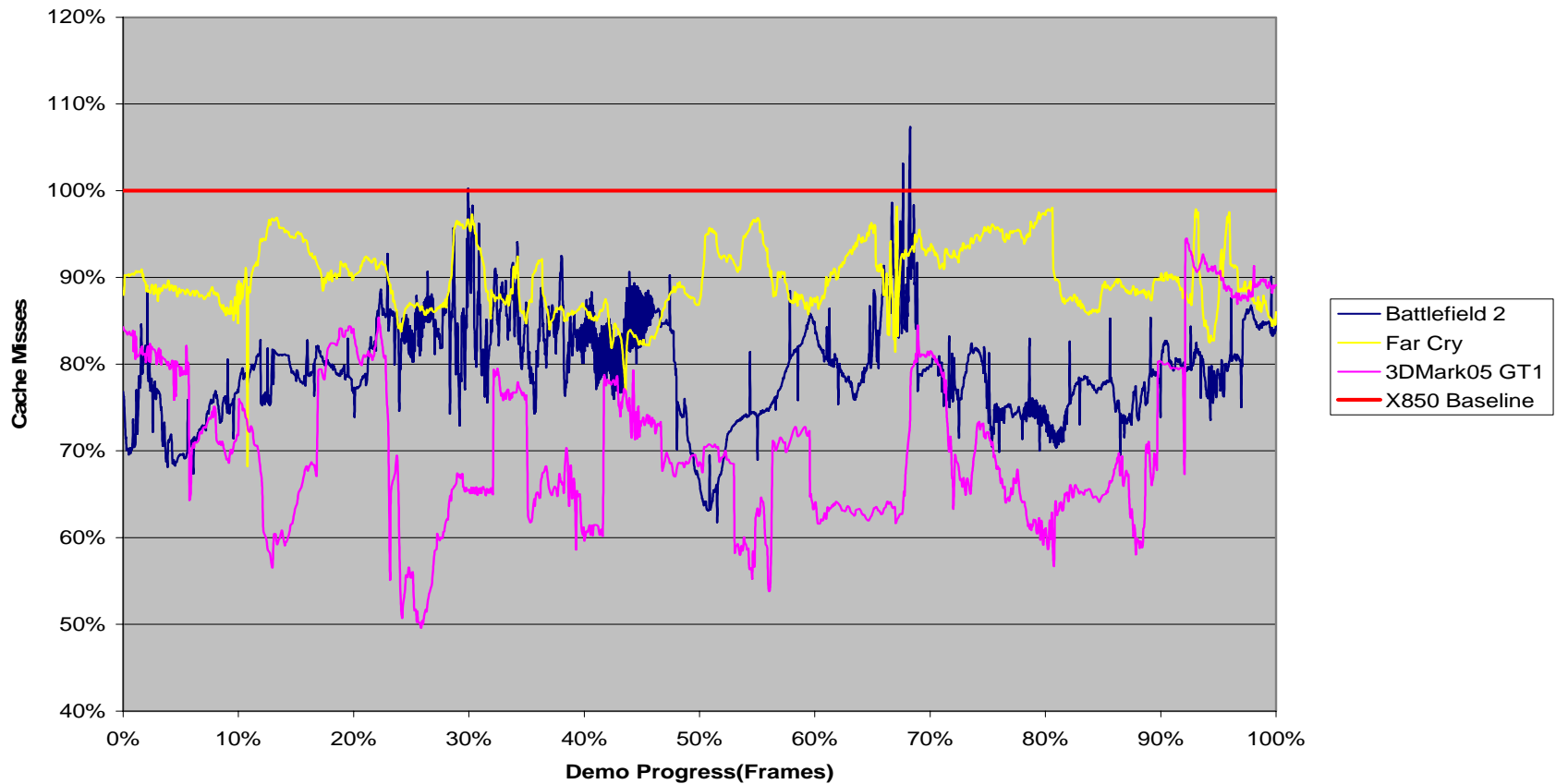
### Fully Associative Cache



# Cache Performance



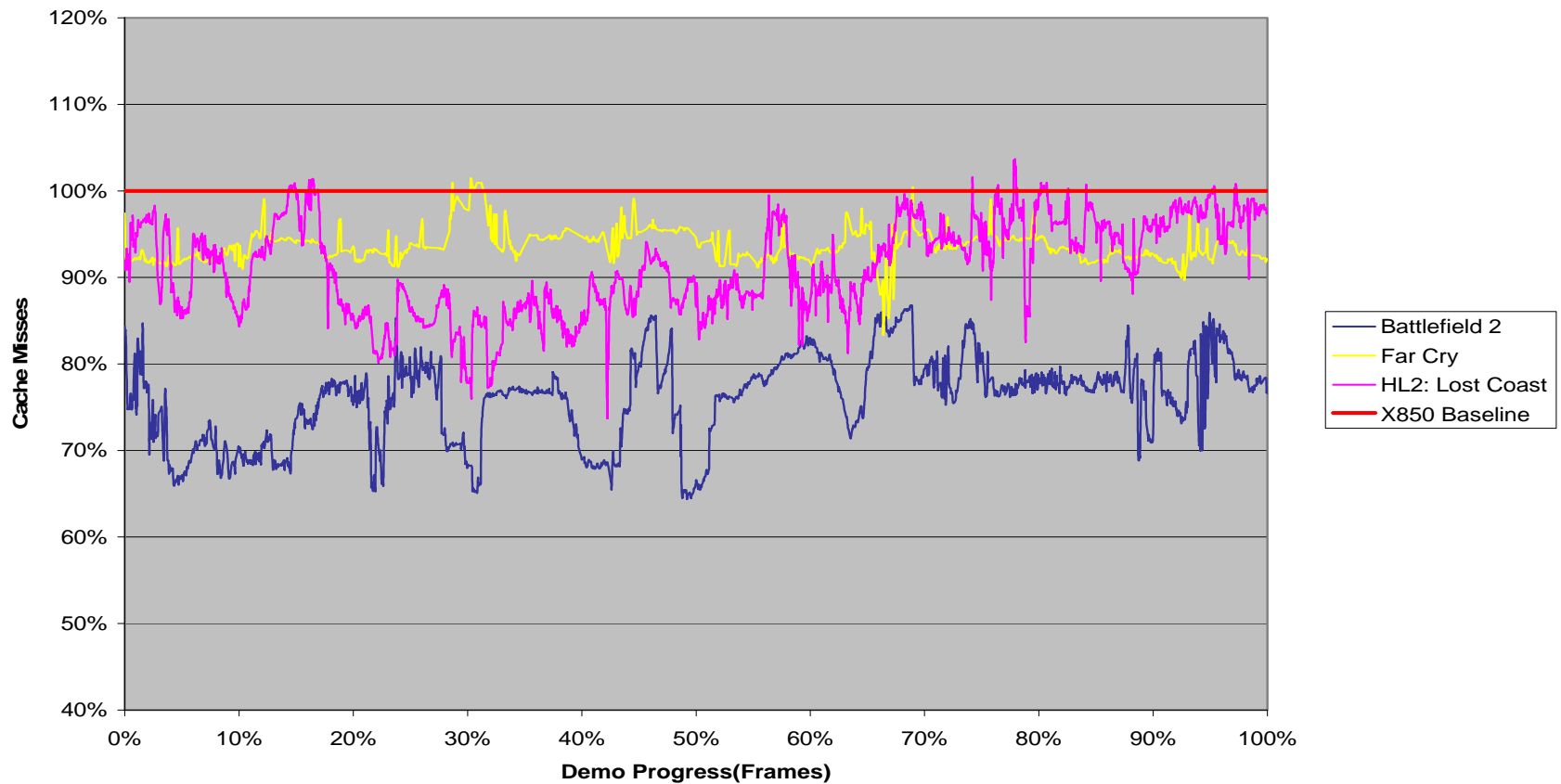
X1800 Z Cache Misses Relative to X850



# Cache Performance



X1800 Texture Cache Misses Relative to X850

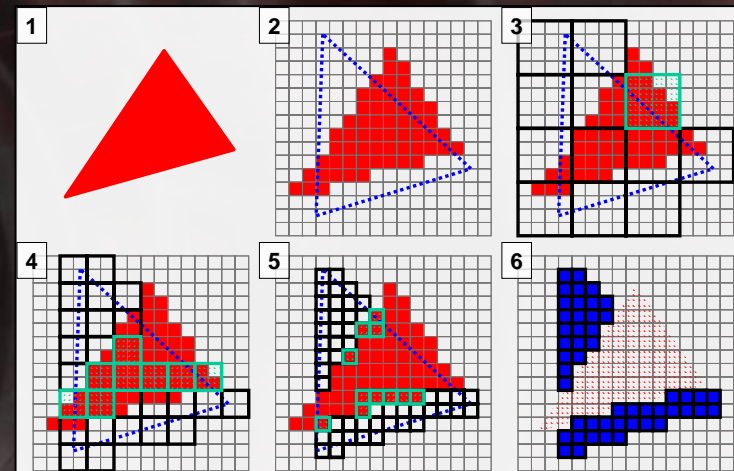


# Hyper Z



## Improved Hierarchical Z Buffer

- Detects and discards hidden pixels before shading
- Important in scenes with heavy overdraw (i.e. overlapping objects)
- New technique uses floating point for improved precision
- Catches up to 60% more hidden pixels than X850



## Improved Z Compression

- Z Buffer data is typically the largest user of memory bandwidth
- Bandwidth can be reduced by up to 8:1 using lossless compression
- New method achieves higher compression ratios more often

# Memory Controller Performance



- New technology benefits most apparent in most bandwidth-demanding situations
  - High resolutions (1600x1200 and up)
  - Anti-Aliasing (4x and 6x modes, Adaptive AA)
  - Anisotropic Filtering (8x and 16x Quality AF modes)
- Frame rates over 2x faster than previous generation in these cases

# Anti-Aliasing Performance



Far Cry - Regulator



# Anti-Aliasing Performance



Battlefield 2

